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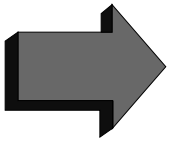
SONET/SDH and ATM The Local Area Network Agenda



- **Section 1: Physical layers for ATM***
- **Section 2: SONET**/SDH*** as a physical layer for ATM**
- **Section 3: ATM**
- **Section 4: ATM and related protocols**
- **Section 5: TI™ solutions**

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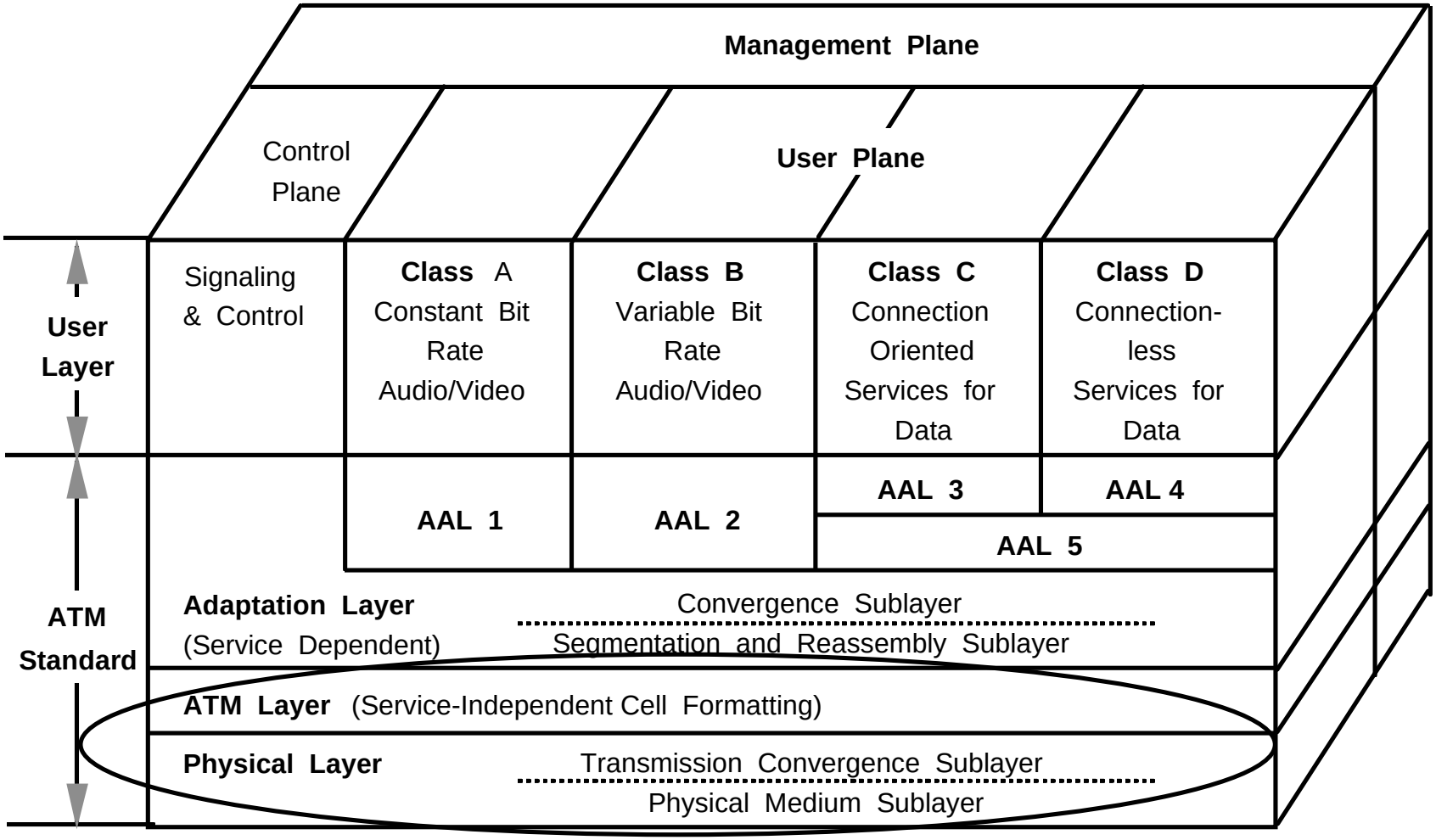
B - ISDN REFERENCE MODEL



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FUNCTIONS OF THE ATM LAYERS

LAYER MANAGEMENT	HIGHER LAYER FUNCTIONS	HIGHER LAYER	
	Convergence Sublayer	CS	AAL
	Segmentation and Reassembly	SAR	AAL
	Generic Flow Control Cell Header Generation/Extraction Cell VPI/VCI Translation Cell Multiplex and Demultiplex	ATM	
	Cell Rate Decoupling HEC Sequence Generation/Verification Cell Delineation Transmission Frame Adaptation Transmission Frame Generation/Recovery	TC	Physical Layer
	Bit Timing Physical Medium Dependent	PMD	Physical Layer

UTOPIA Interface

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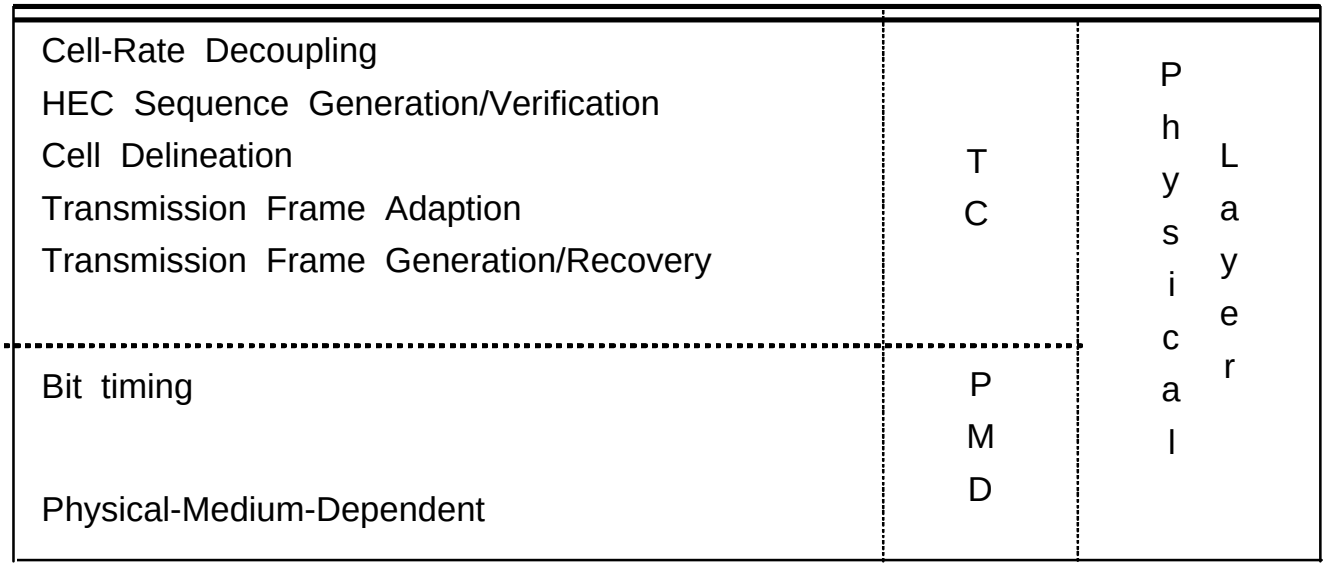
Two Sublayers



- **PMD:**
  - **Medium line code connectors**
  - **Probably use existing standards and technology**
- **TCS:**
  - **Specific to the PMD**
  - **Cell delineation**
  - **Cell-rate decoupling (inserting empty cells during idle periods**

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UTOPIA Levels 1 and 2

- **Universal Test and Operations PHY Interface for ATM**
  - **Allows a common, standard interface between ATM (SARs) and PHY layers of ATM subsystems**
  - **Features three different clock rates: 25-MHz/8-bit interface, 33-MHz/8- or 16-bit interface, and 50-MHz/16-bit interface**
  - **Multiple operation allows the SAR to control multiple physical layer devices**

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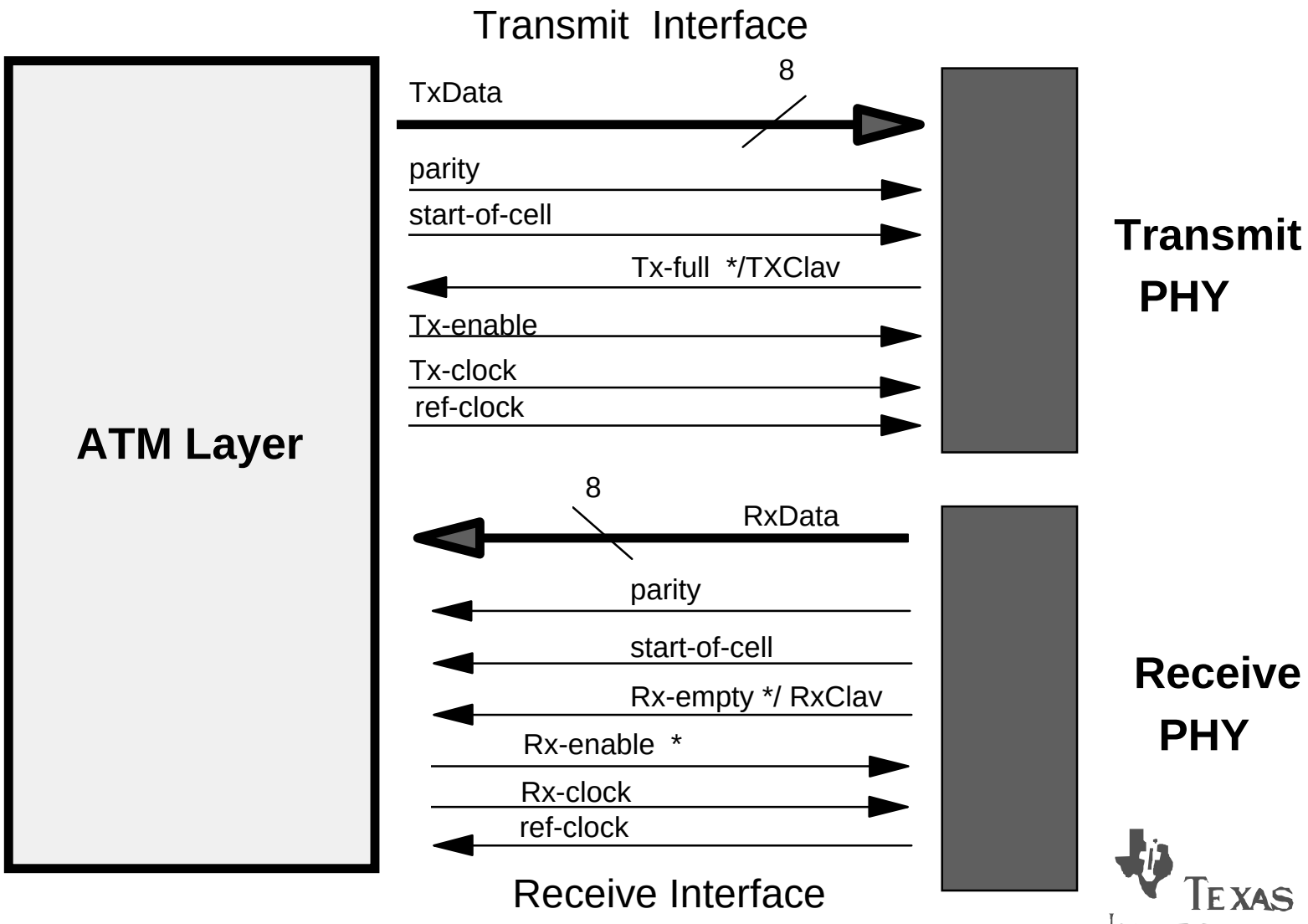
UTOPIA Interface Block Diagram



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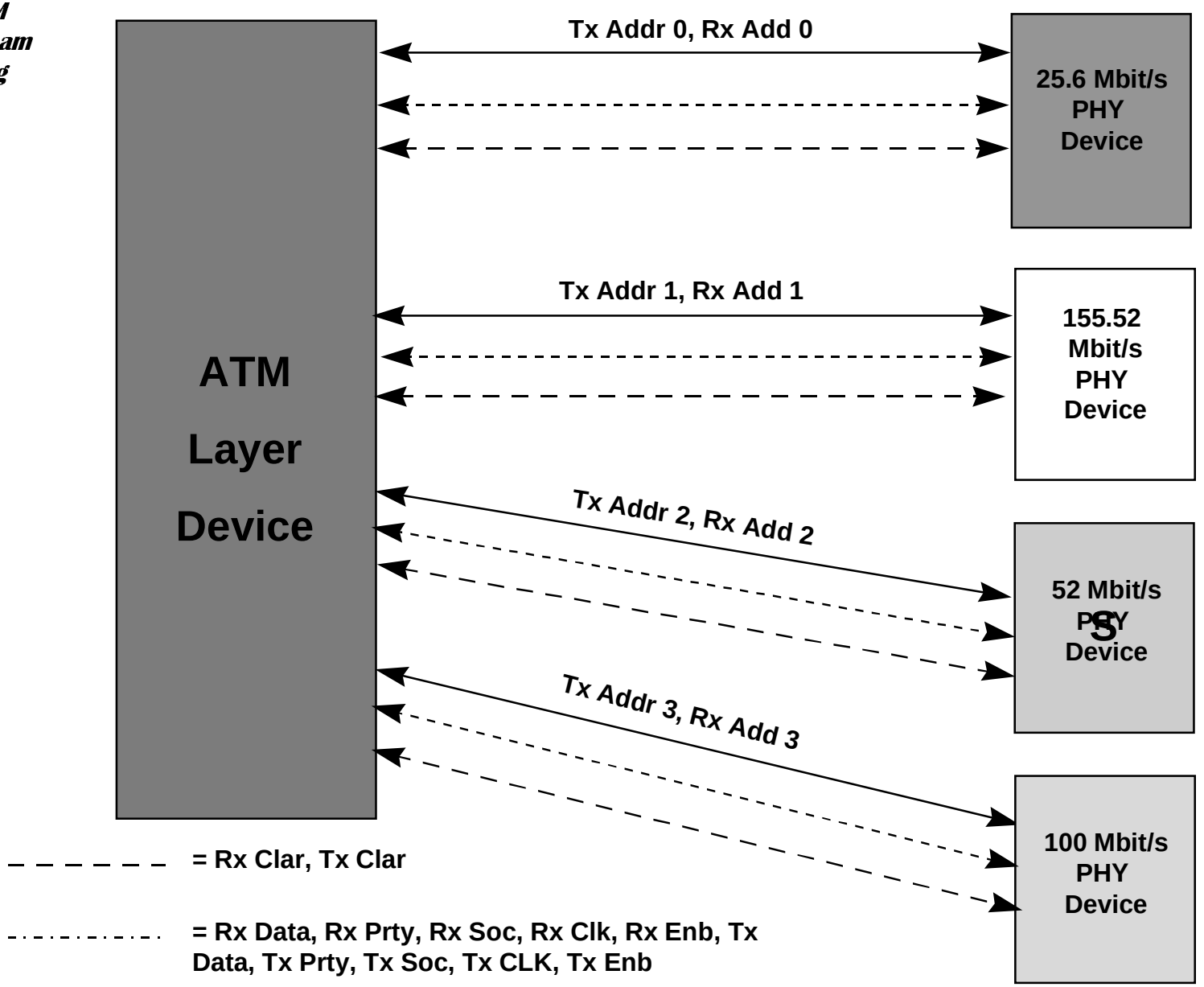
UTOPIA 2 Interface



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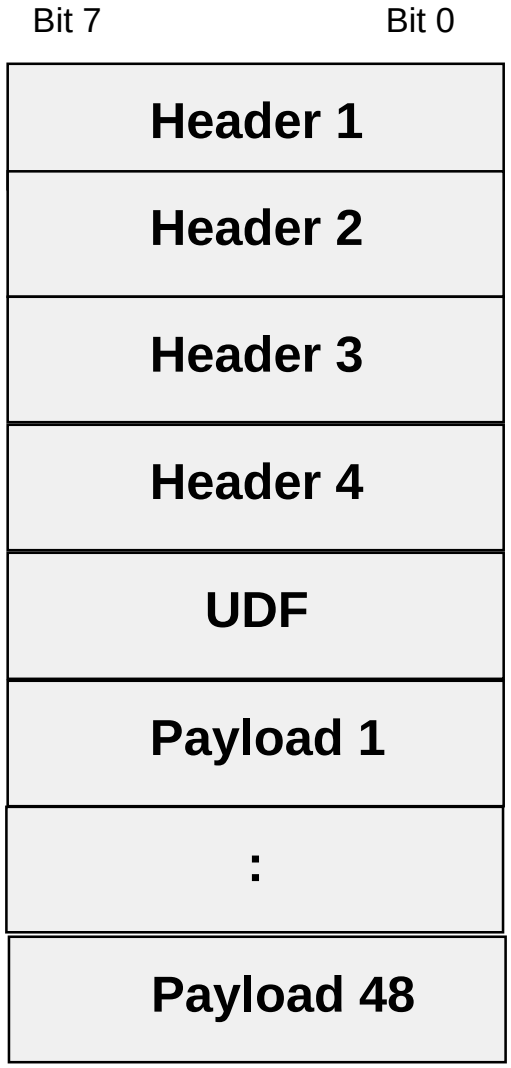
UTOPIA
Cell format 8-bit mode



UDF = User defined (e.g., HEC)

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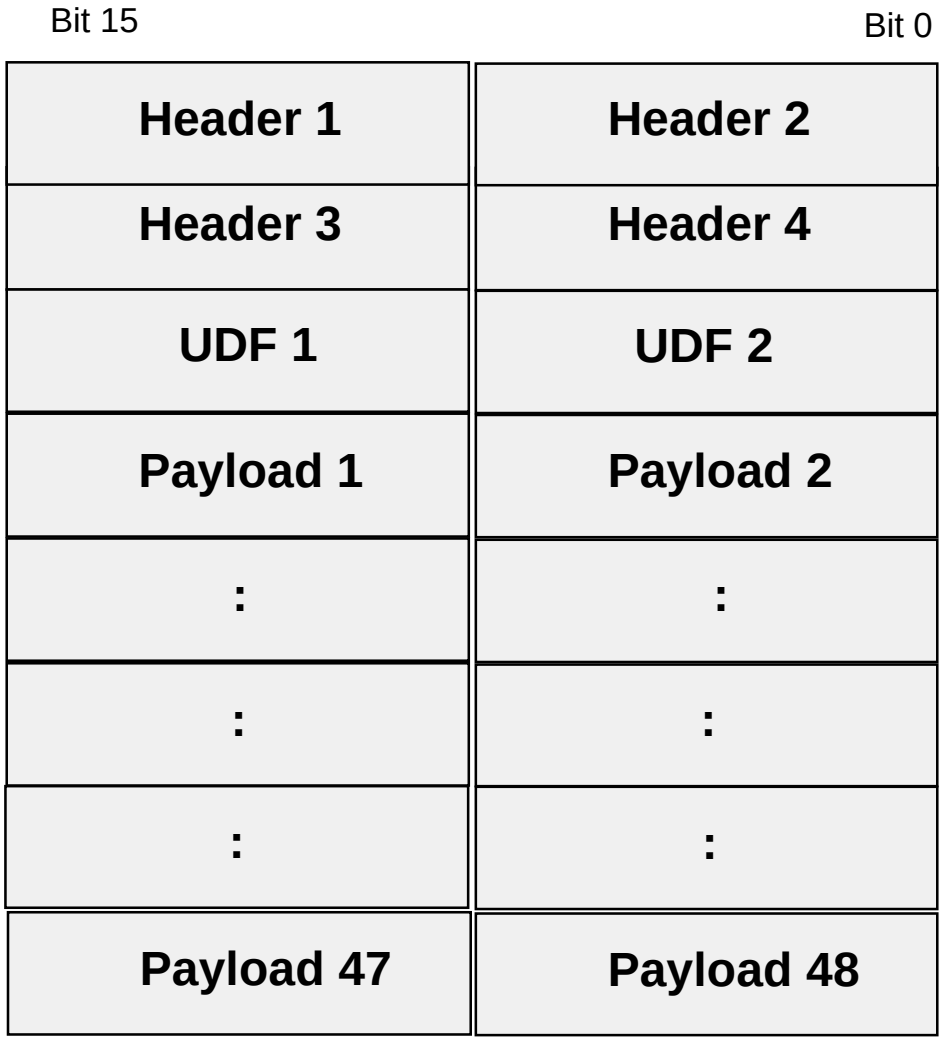
UTOPIA
Cell format 16-bit mode



UDF = User defined (e.g., HEC)

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Private UNI

ATM Forum Physical Layer UNI Interfaces		
Frame Format	**Bit Rate/Line Rate**	**Transmission Media**
Cell Stream	25.6 Mbit/s/32 Mbaud	UTP-3
STS-1	51.84 Mbit/s	UTP-3
FDDI	100 Mbit/s/125 Mbaud	MMF
STS-3c, STM-1	155.52 Mbit/s	UTP-5
STS-3c, STM-1	155.52 Mbit/s	SMF, MMF, Coax pair
Cell Stream	155.52 Mbit/s/194.4 Mbaud	MMF/STP
STS-3c, STM-1	155.52 Mbit/s	UTP-3
STS-12, STM-4	622.08 Mbit/s	SMF, MMF

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Public UNI

ATM Forum Physical Layer UNI Interfaces		
Frame Format	**Bit Rate**	**Transmission Media**
DS1	1.544 Mbit/s	Twisted Pair
DS3	44.736 Mbit/s	Coax Pair
STS-3c, STM-1	155.520 Mbit/s	SMF
E1	2.048 Mbit/s	Twisted Pair, Coax Pair
E3	34.368 Mbit/s	Coax Pair
J2	6.312 Mbit/s	Coax Pair
N X T1	N X 1.544 Mbit/s	Twisted Pair

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Driving ATM Into Mainstream Networking

SONET/SDH and ATM The Local Area Network Agenda

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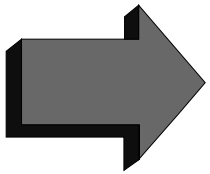
Driving ATM Into Mainstream Networking

SONET/SDH as a Physical Layer for ATM



- Standards bodies and standard rates
- The four layers of SONET/SDH
- Terminating equipment
- Frame structure
- Overhead bytes
- SONET/SDH mapping for ATM
- Differences between SONET and SDH

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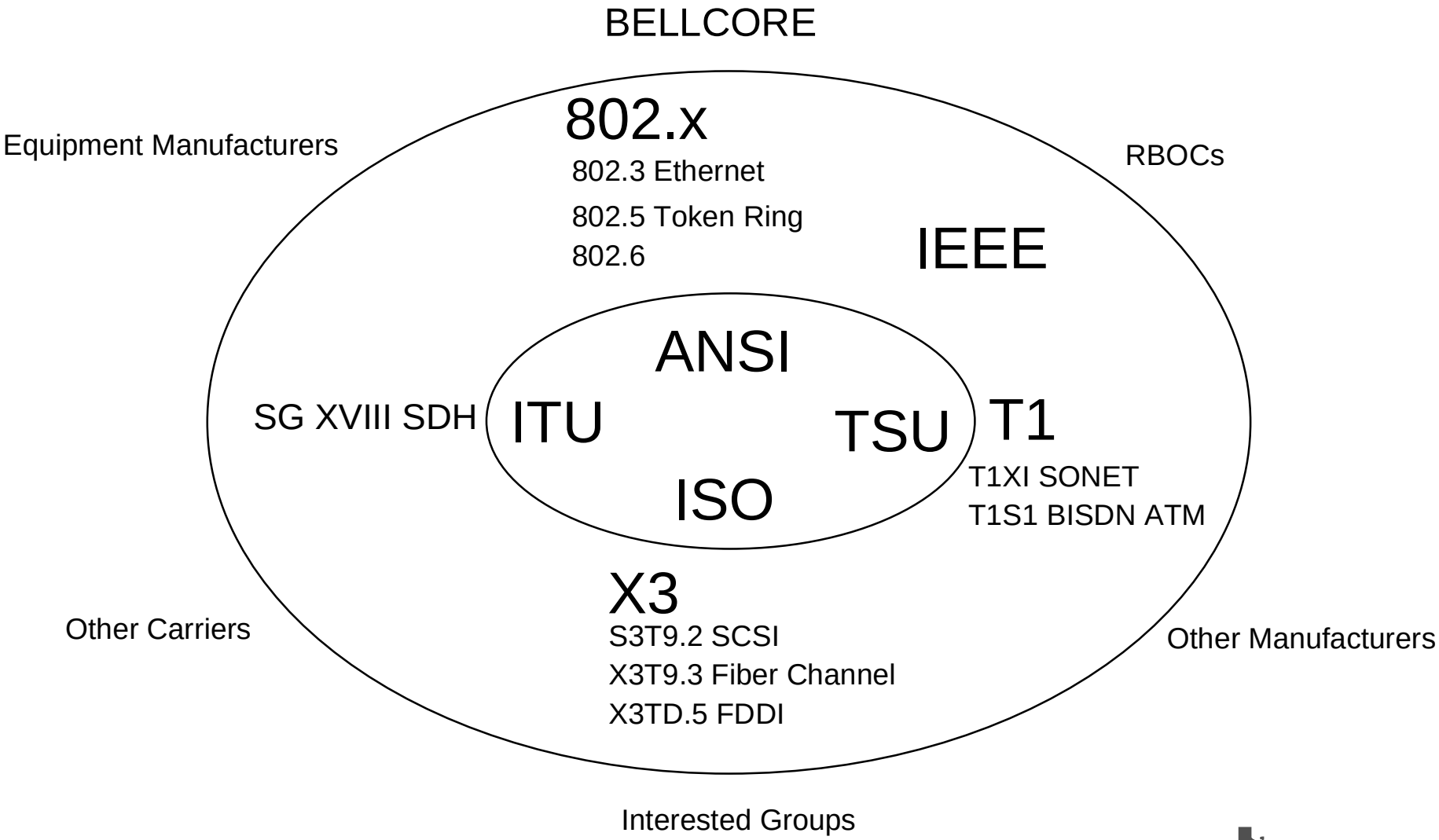
International Standards Bodies



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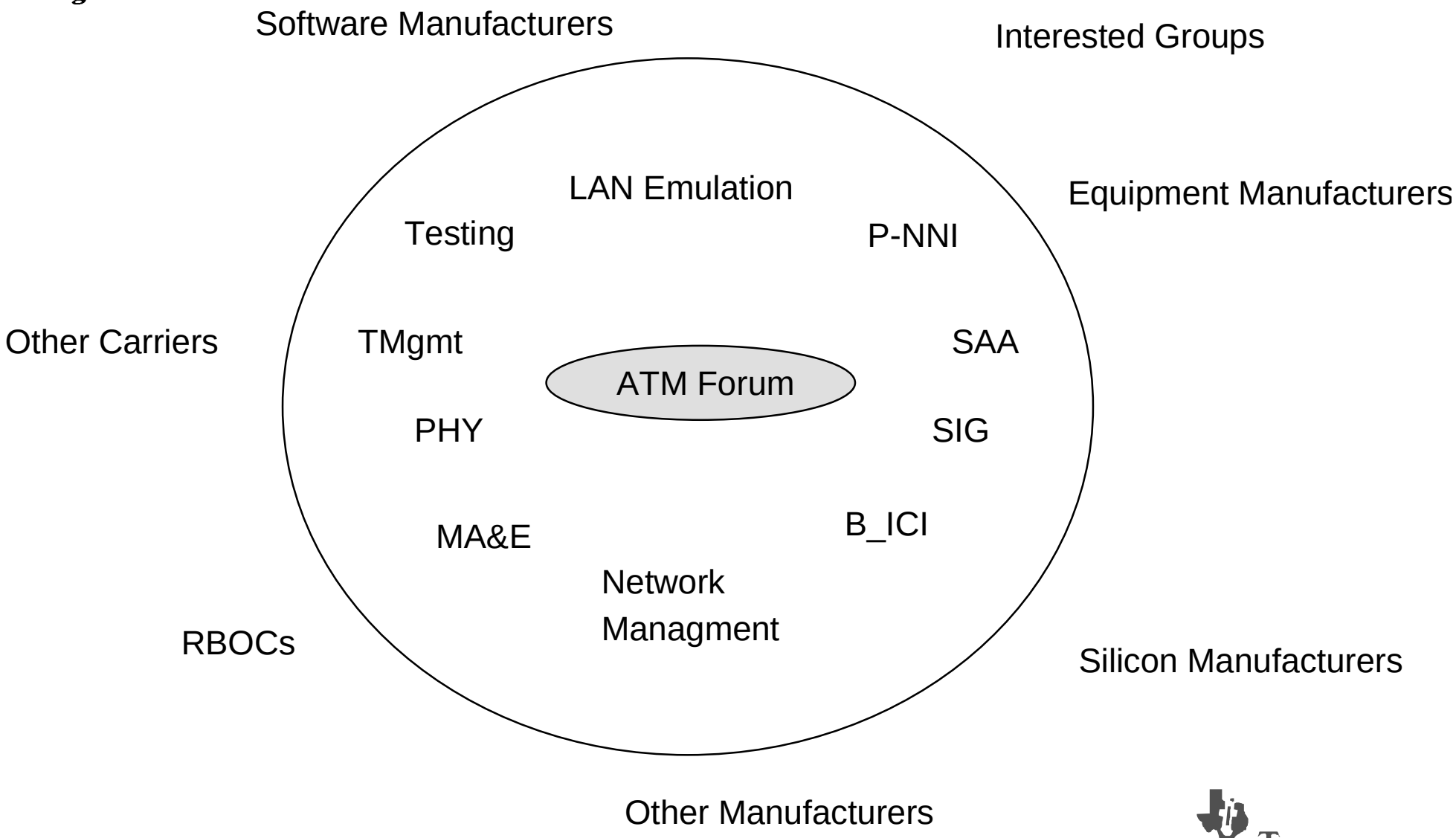
The ATM Forum



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SONET/SDH

- Common standard toward which multiple vendors can build equipment
- Supports interoperability "at the mid-span meet"
- Compatible fiber-optic transmission systems (FOTS) mean competition and lower costs
- Better operations and support management (OSS)
- Fast provisioning of bandwidth
- New circuits can be software defined and updated from a distance
- Easy extraction of lower-rate signals from the payload
- Better network survivability
- Primary and backup pair of fiber-optic cabling between nodes
- 60 ms or less S/W rerouting capability
- Support future services
- HDTV, CAD/CAM, WAN backbone, BISDN
- Improved capability to transport other types of information besides voice

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SONET/SDH Line Rates

Data Rate (Mbit/s)	SDH Level ITU	Optical Carrier Level	SONET Level ANSI*
51.840		OC-1	STS-1
155.520	STM-1	OC-3	STS-3c
622.080	STM-4	OC-12	STS-12
1.244160 Gbit/s	STM-8	OC-24	STS-24
2.488320 Gbit/s	STM-16	OC-48	STS-48
N * 51.84 Mbit/s	STM-M	OC-N	STS-N

SONET: Synchronous optical network
SDH: Synchronous digital hierarchy
* Electrical carrier
M=N/3

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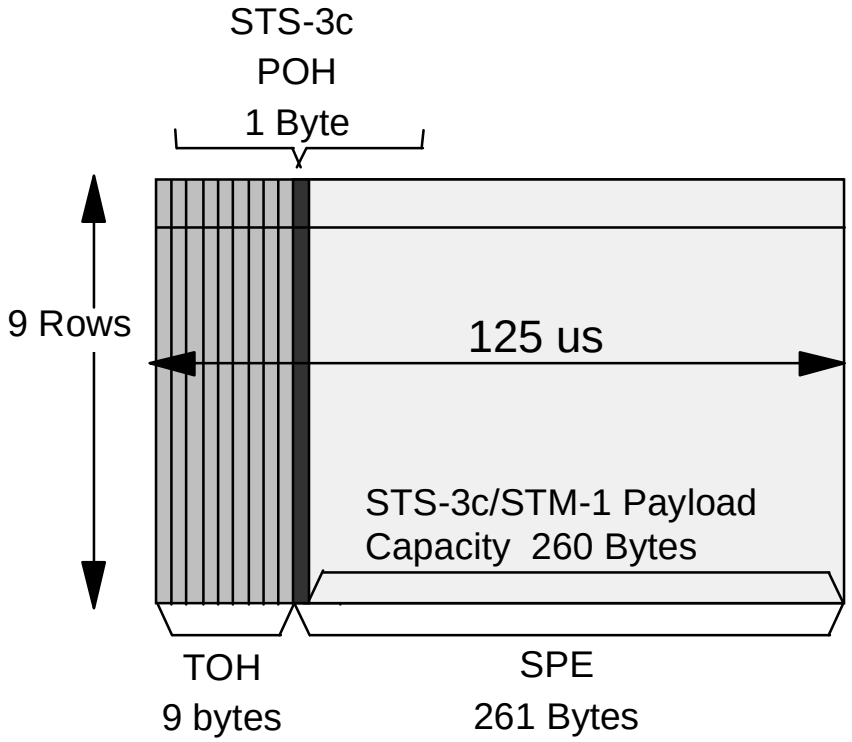
Why a SONET/SDH Frame Every 125 µs?

- **Bandwidth for voice = 4 kHz**
  - **8,000 samples/s**
  - **1/8,000 = 125 µs**
  - **SONET/SDH frame every 125 µs**
  - **Many ATM cells every 125 µs**
  - **[8,000 samples/s] [8 bits/sample] = 64 kbit/s**
- **One voice channel = 64 kbit/s (DS0 rate), the basic building block of U.S. public voice network**

SONET/SDH Payload Calculation



Each STS-3c/STM-1 frame provides 155.52 Mbit/s. 90 bytes of the 2430 bytes are used by the transport overhead (TOH) and path overhead (POH), which leaves 2340 bytes (96.3% of the SONET/SDH frame) for the payload. The amount of SONET/SDH payload available in an STS-3c/STM-1 frame =150 Mbit/s.

≈ **150 Mbit/s**

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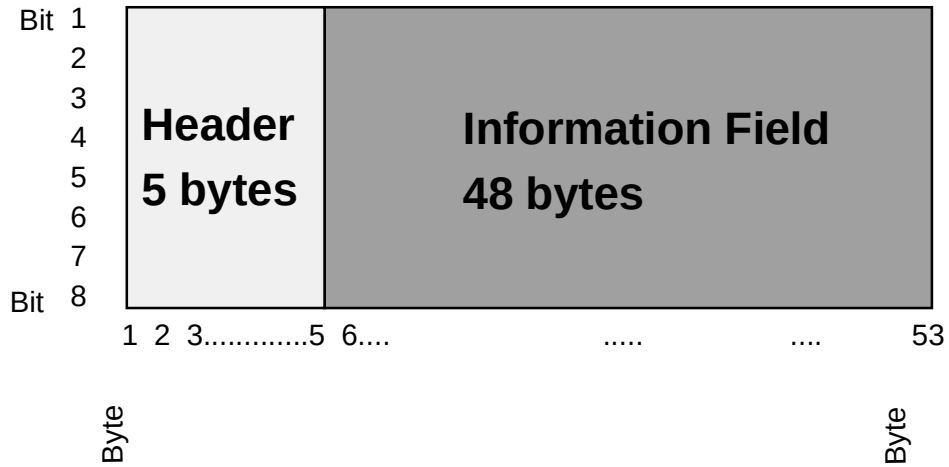
SONET/SDH PAYLOAD CALCULATION



90 % of the ATM cell is available for user information. If an ATM cell is inserted into a SONET/SDH frame, what bandwidth is available for user information?

$$\frac{[2340 \text{ payload bytes/frame} - ((5 \text{ ATM overhead bytes/cell})(44 \text{ cells/frame}))][155 \text{ Mbit/s}]}{2430 \text{ total bytes/frame}} \approx \textbf{135 Mbit/s}$$

An STS-3c/STM-1 frame has a data rate of 155 Mbit/s. The maximum usable data rate for user information is 135 Mbit/s; this excludes any AAL processing. If AAL processing is necessary, the data rate is reduced below 135 Mbit/s.

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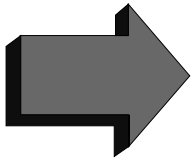
Driving ATM Into Mainstream Networking

SONET/SDH as a Physical Layer for ATM



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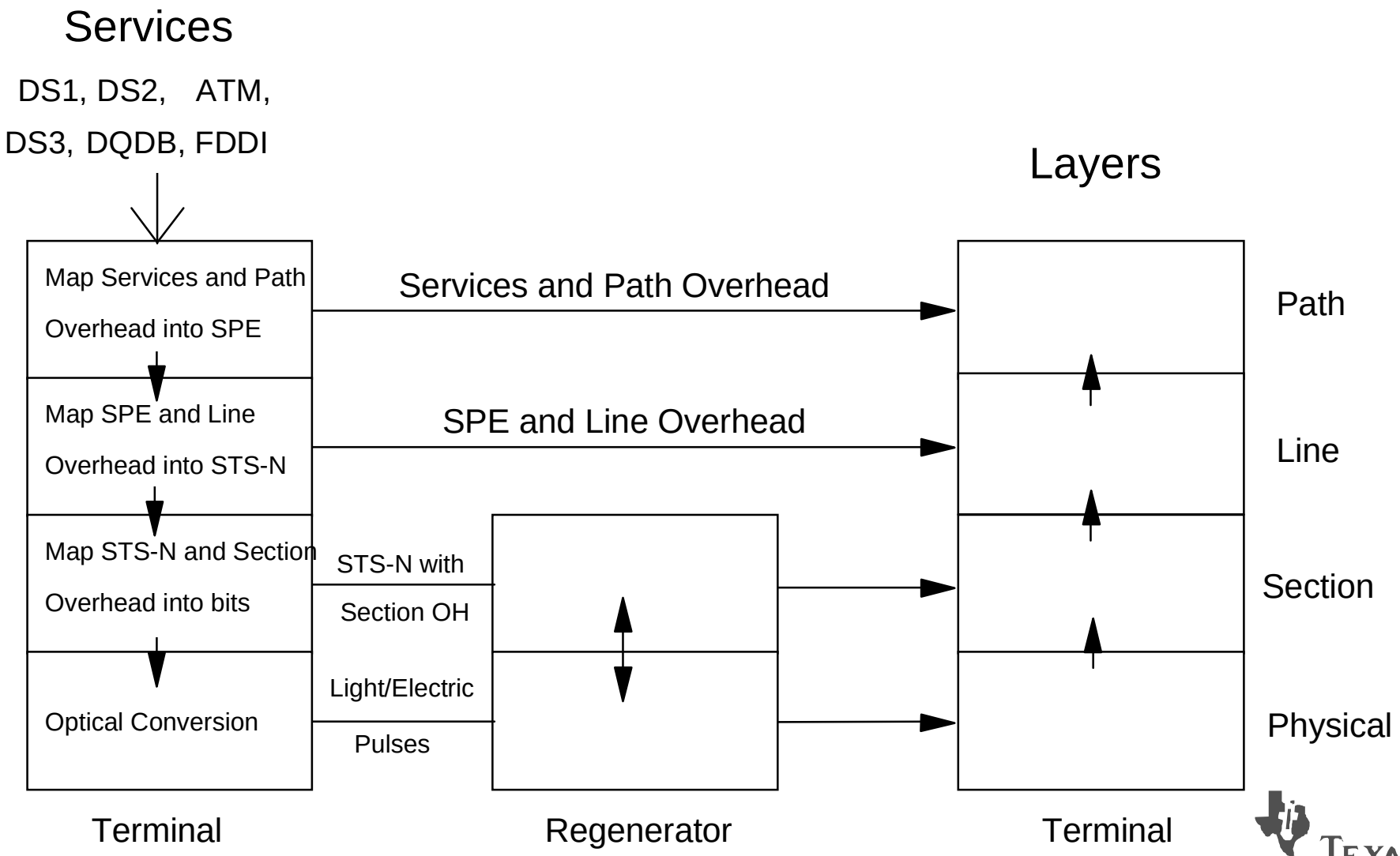
Driving ATM Into Mainstream Networking

The Four Layers of SONET/SDH



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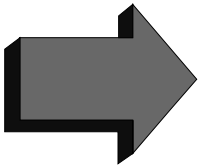
SONET/SDH as a Physical Layer for ATM



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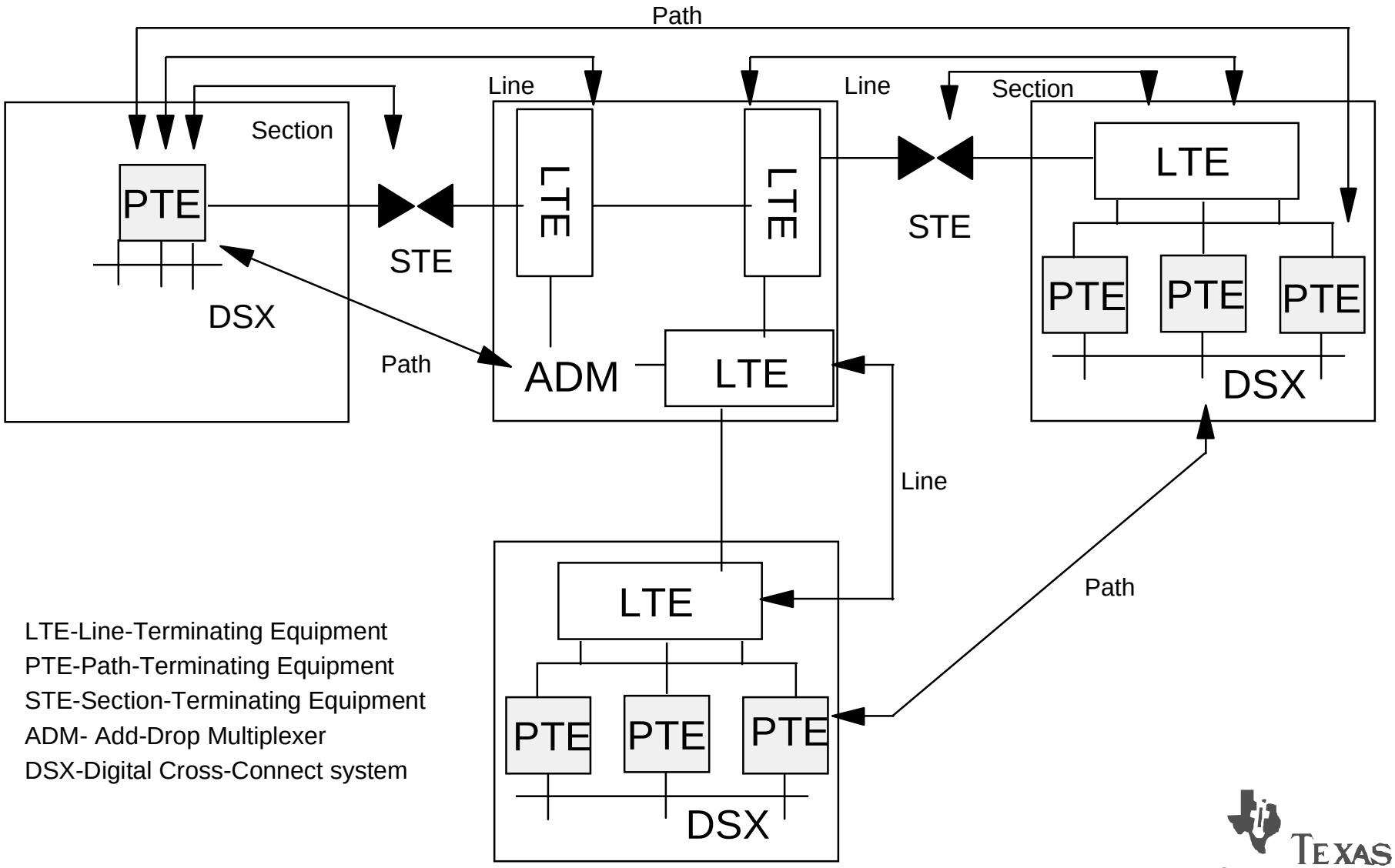
Section, Line, and Path (the big picture)



LTE-Line-Terminating Equipment
PTE-Path-Terminating Equipment
STE-Section-Terminating Equipment
ADM- Add-Drop Multiplexer
DSX-Digital Cross-Connect system

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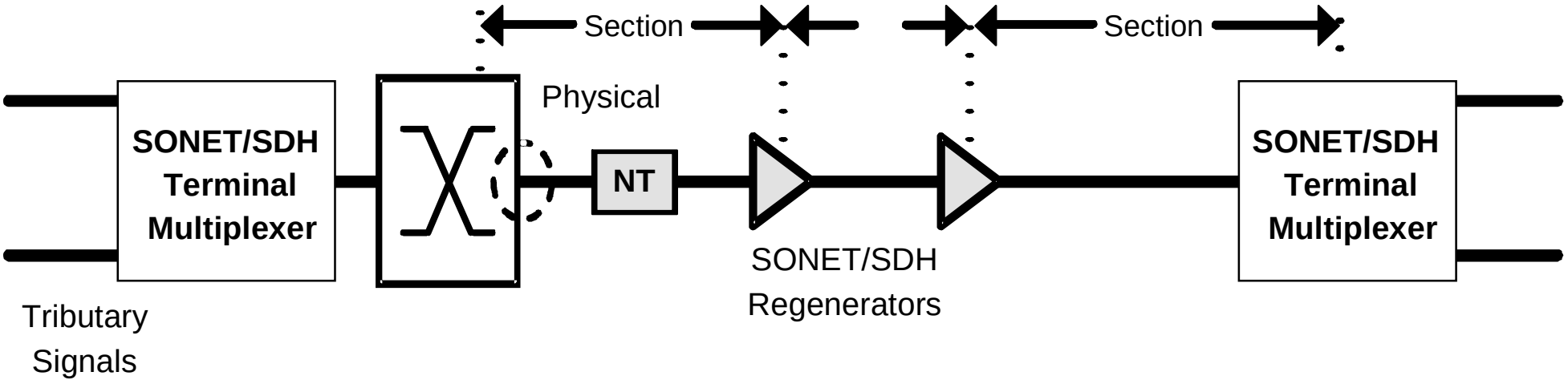
Definition of SONET/SDH Network Section



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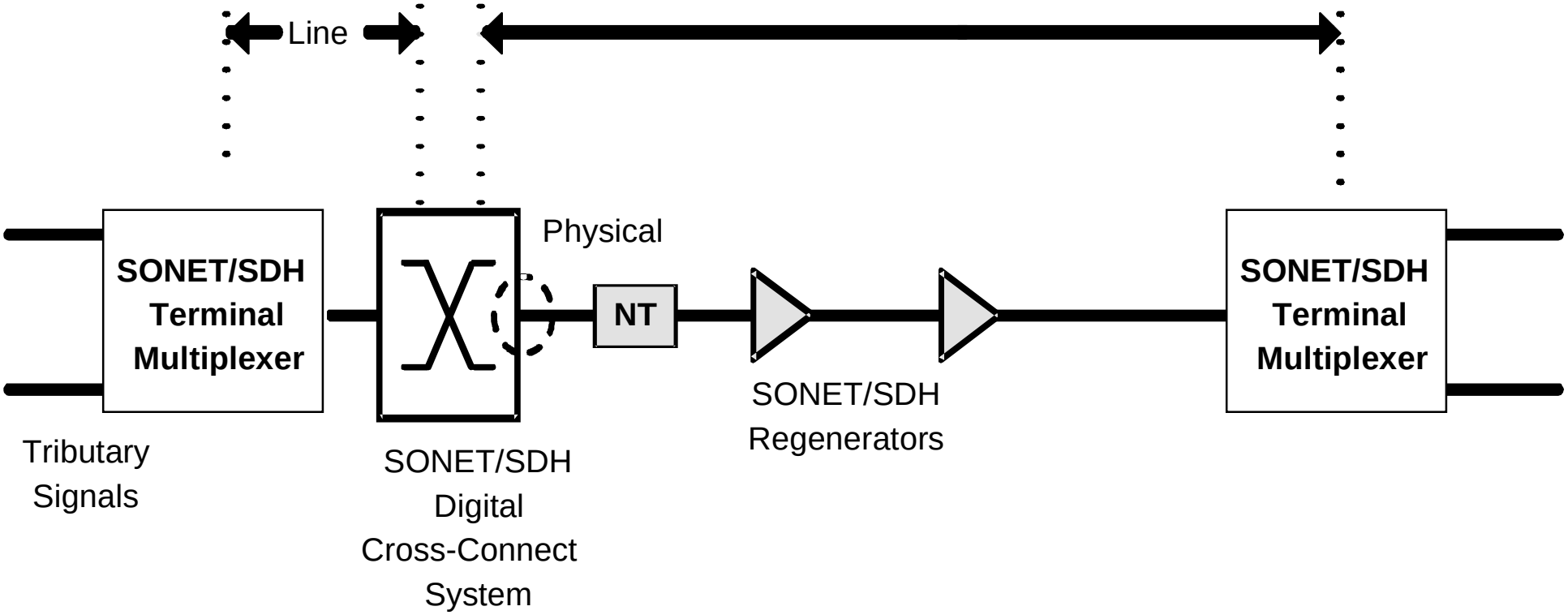
Definition of SONET/SDH Network Line



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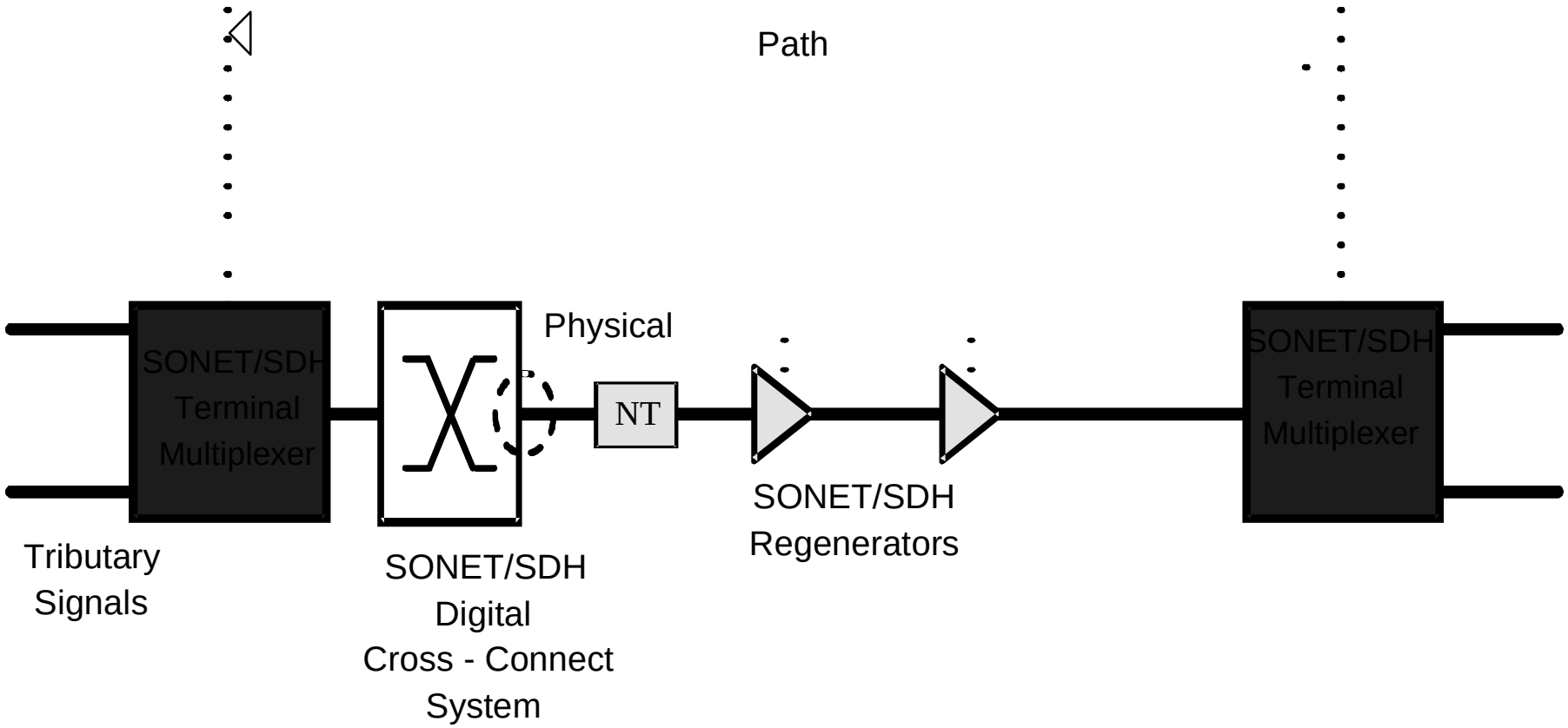
Definition of SONET Network Path



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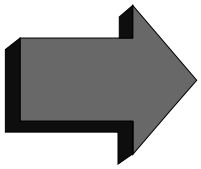
SONET as a Physical Layer for ATM



- Standards bodies
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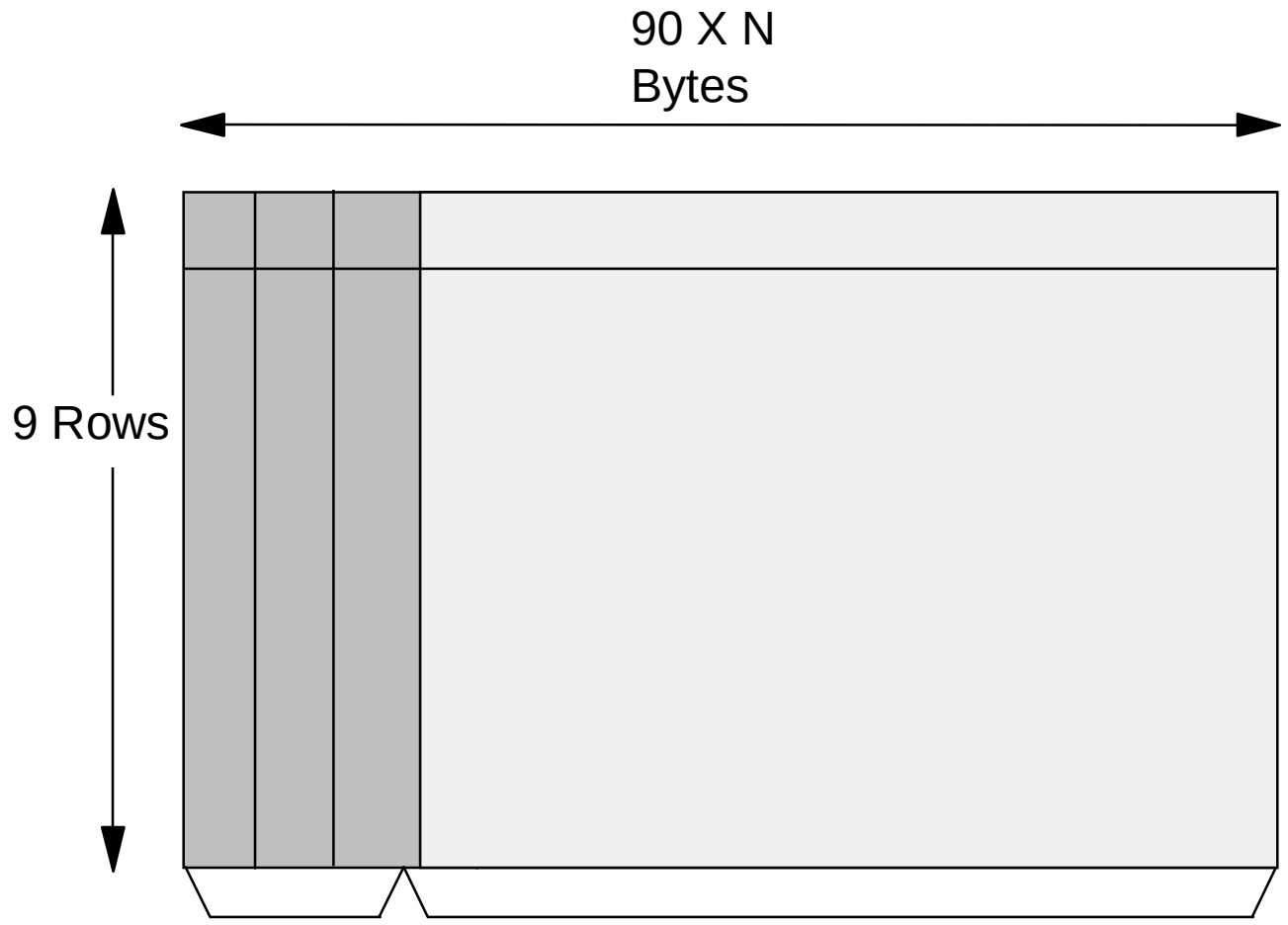
Generic Frame Structure for STS-N/STM-M



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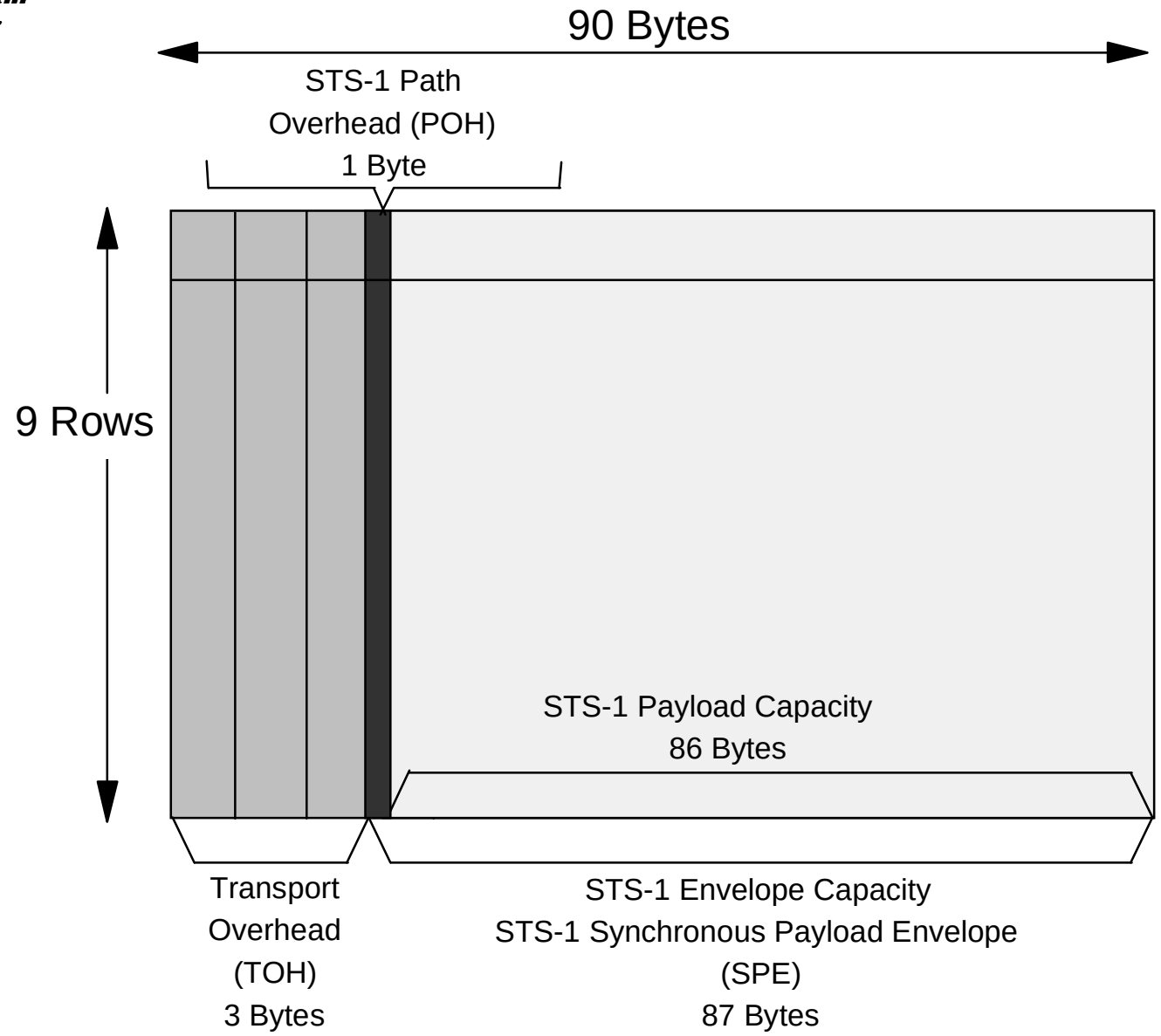
Frame Structure for STS-1



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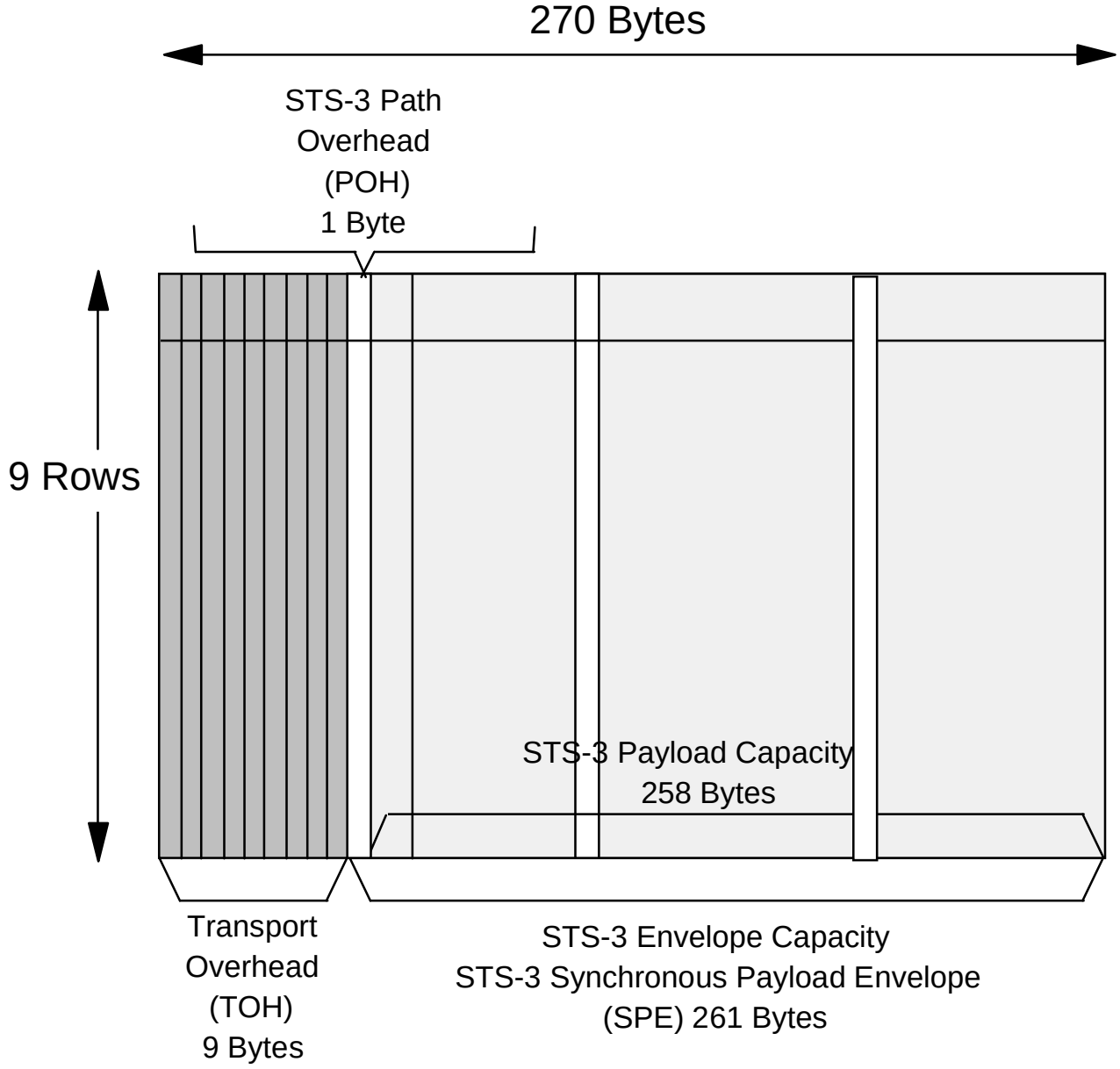
Frame Structure of STS-3



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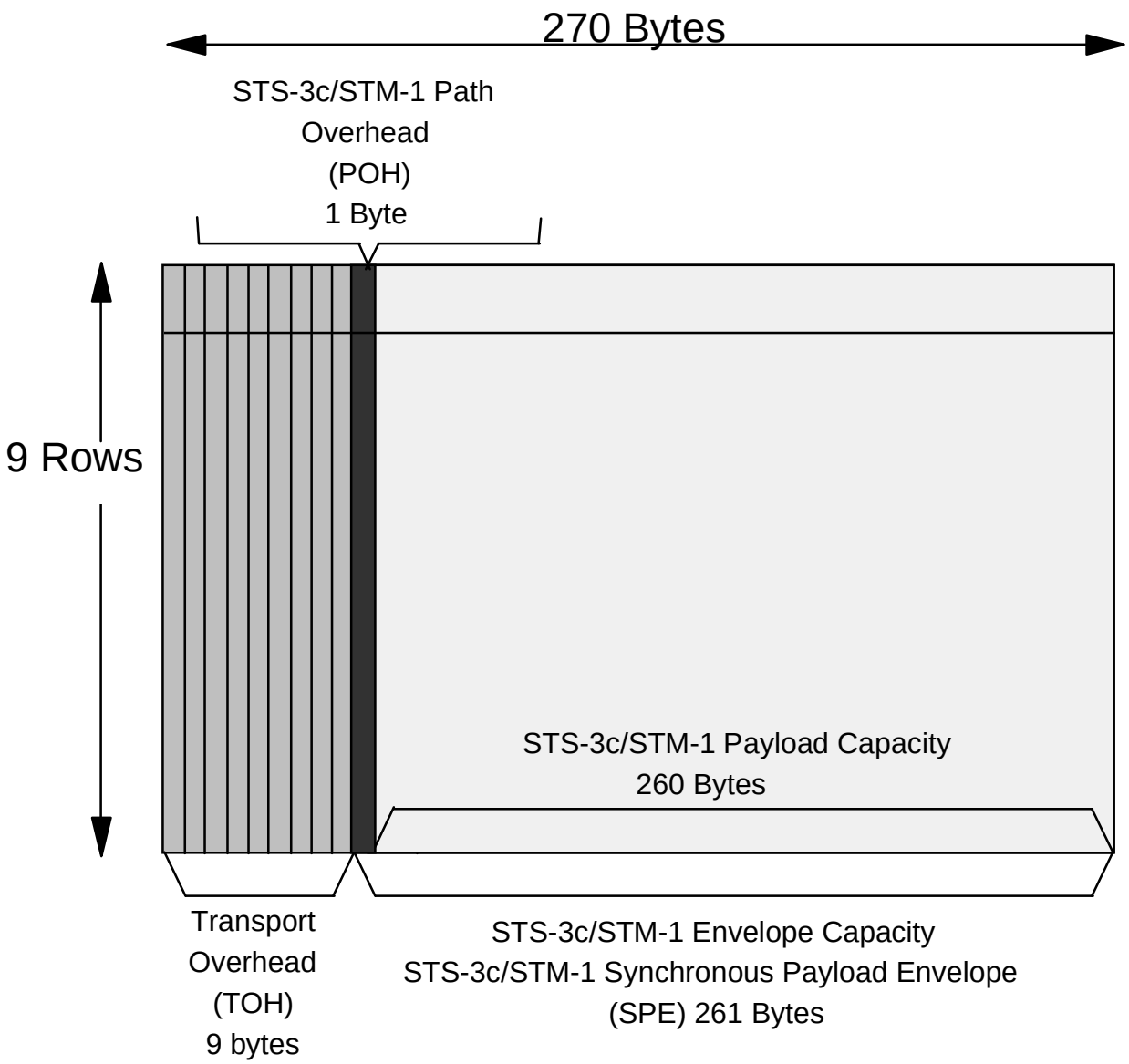
Frame Structure of STS-3c/STM-1



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Driving ATM Into Mainstream Networking

SONET/SDH as a Physical Layer for ATM

- Standards bodies
- The four layers of SONET/SDH
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SONET/SDH Frame Structure

Section Overhead	Framing A1	Framing A1	Framing A1	Framing A2	Framing A2	Framing A2	STS-1 ID C1	STS-1 ID C1	STS-1 ID C1
	BIP-8 B1	BIP-8 B1	BIP-8 B1	Orderwire E1	Orderwire E1	Orderwire E1	User F1	User F1	User F1
	Data Com D1	Data Com D1	Data Com D1	Data Com D2	Data Com D2	Data Com D2	Data Com D3	Data Com D3	Data Com D3
Line Overhead	Pointer H1	Pointer H1	Pointer H1	Pointer H2	Pointer H2	Pointer H2	Pointer/Action H3	Pointer/Action H3	Pointer/Action H3
	BIP-8 B2	BIP-8 B2	BIP-8 B2	APS K1	APS K1	APS K1	APS K2	APS K2	APS K2
	Data Com D4	Data Com D4	Data Com D4	Data Com D5	Data Com D5	Data Com D5	Data Com D6	Data Com D6	Data Com D6
	Data Com D7	Data Com D7	Data Com D7	Data Com D8	Data Com D8	Data Com D8	Data Com D9	Data Com D9	Data Com D9
	Data Com D10	Data Com D10	Data Com D10	Data Com D11	Data Com D11	Data Com D11	Data Com D12	Data Com D12	Data Com D12
	Growth Z1	Growth Z1	Growth Z1	Growth/FEBE Z2	Growth/FEBE Z2	Growth/FEBE Z2	Orderwire E2	Orderwire E2	Orderwire E2

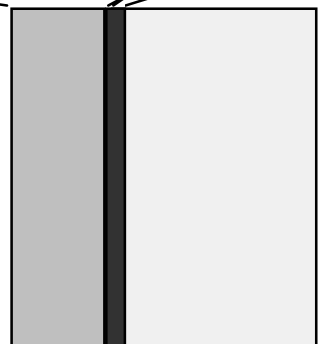
Transport Overhead

Path Overhead
Trace J1
BIP-8 B3
Signal Label C2
Path Status G1
User Channel F2
Indicator H4
Growth/DQDB Z3
Growth Z4
Growth Z5

Calculated by SABRE

Constant Values

STS-3c/STM-1 Frame Overhead



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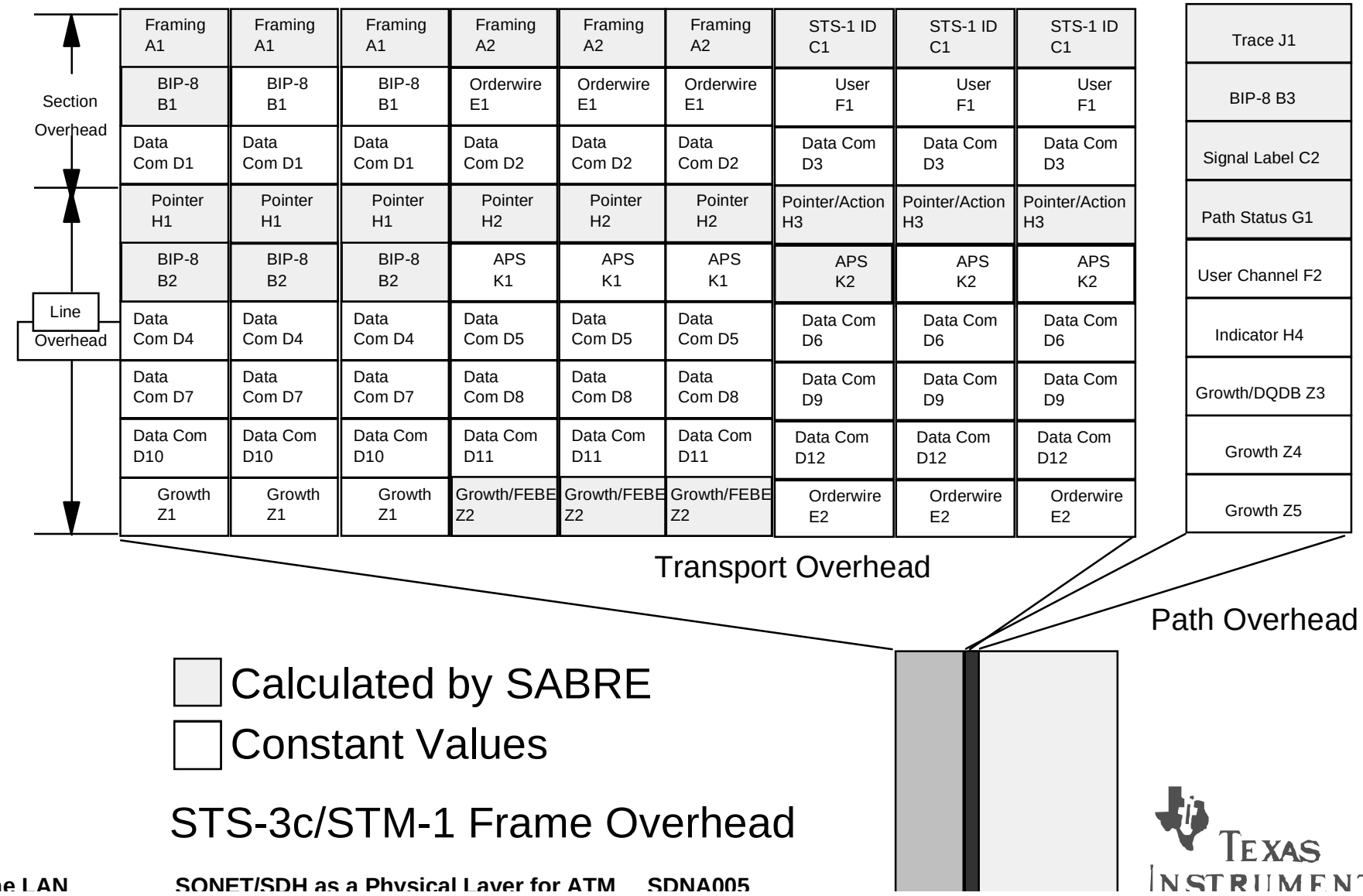
Overhead bytes used in the Public UNI



STS-3c/STM-1 Frame Overhead

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STS-3c/STM-1 Section Overhead

	SONET			SDH		
Section Overhead	1st Value	2nd Value	3rd Value	1st Value	2nd Value	3rd Value
A1	1111 0110	1111 0110	1111 0110	1111 0110	1111 0110	1111 0110
A2	0010 1000	0010 1000	0010 1000	0010 1000	0010 1000	0010 1000
C1	0000 0001	0000 0010	0000 0011	0000 0001	0000 0000	0000 0000
B1	Calculated	Calculated	Calculated	Calculated	Calculated	Calculated
E1	Provides Local Channel	Provides Local Channel	Provides Local Channel	Provides Local Channel	Provides Local Channel	Provides Local Channel
F1	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
D1	Provide a data Communications Channel @ 192kb/its	Provide a data Communications Channel @ 192kbit/s	Provide a data Communications Channel @ 192kbit/s	Provide a data Communication s Channel @ 192kbit/s	Provide a data Communication s Channel @ 192kbit/s	Provide a data Communication s Channel @ 192kbit/s
D2	Provide a data Communications Channel @ 192kbit/s	Provide a data Communications Channel @ 192kbit/s	Provide a data Communications Channel @ 192kbit/s	Provide a data Communication s Channel @ 192kbit/s	Provide a data Communication s Channel @ 192kbit/s	Provide a data Communication s Channel @ 192kbit/s
D3	Provide a data Communications Channel @ 192kbit/s	Provide a data Communications Channel @ 192kbit/s	Provide a data Communications Channel @ 192kbit/s	Provide a data Communication s Channel @ 192kbit/s	Provide a data Communication s Channel @ 192kbit/s	Provide a data Communication s Channel @ 192kbit/s

☐ Calculated by Physical Layer

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Driving ATM Into Mainstream Networking

STS-3c/STM-1 Line Overhead

	SONET			SDH		
Line Overhead	1st Value	2nd Value	3rd Value	1st Value	2nd Value	3rd Value
H1	0110 0010	1001 0011	1001 0011	0110 1010	1001 1011	1001 1011
H2	0000 1010	1111 1111	1111 1111	0000 1010	1111 1111	1111 1111
H3	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000
K1	Calculated	Calculated	Calculated	Calculated	Calculated	Calculated
B2	**Calculated**	**Calculated**	**Calculated**	**Calculated**	**Calculated**	**Calculated**
K2	**Normal = 0000 0000 Line AIS = 0000 0111 Line FERF = 0000 0110**	**Normal = 0000 0000 Line AIS = 0000 0111 Line FERF = 0000 0110**	**Normal = 0000 0000 Line AIS = 0000 0111 Line FERF = 0000 0110**	**Normal = 0000 0000 Line AIS = 0000 0111 Line FERF = 0000 0110**	**Normal = 0000 0000 Line AIS = 0000 0111 Line FERF = 0000 0110**	**Normal = 0000 0000 Line AIS = 0000 0111 Line FERF = 0000 0110**
Z1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Z2	Range of Legal Value is between 0000 0000 and 0001 1000	Range of Legal Value is between 0000 0000 and 0001 1000	Range of Legal Value is between 0000 0000 and 0001 1000	Range of Legal Value is between 0000 0000 and 0001 1000	Range of Legal Value is between 0000 0000 and 0001 1000	Range of Legal Value is between 0000 0000 and 0001 1000
D4-D12	Provide a data Communications Channel @ 576kbit/s	Provide a data Communications Channel @ 576kbit/s	Provide a data Communications Channel @ 576kbit/s	Provide a data Communications Channel @ 576kbit/s	Provide a data Communications Channel @ 576kbit/s	Provide a data Communications Channel @ 576kbit/s

☐ Calculated by Physical Layer

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Driving ATM Into Mainstream Networking

STS-3c/STM-1 Path Overhead

Path Overhead	SONET	SDH
J1	0000 0000	0000 0000
B3	**Calculated from the previous SPE**	**Calculated from the previous SPE**
C2	0001 0011	0001 0011
G1	Path-Termination Status	Path-Termination Status
H4	Multiframe phase indication for VT payload	Multiframe phase indication for VT payload
F2	Reserved	Reserved
Z3-Z5	Reserved	Reserved

☐ Calculated by Physical Layer

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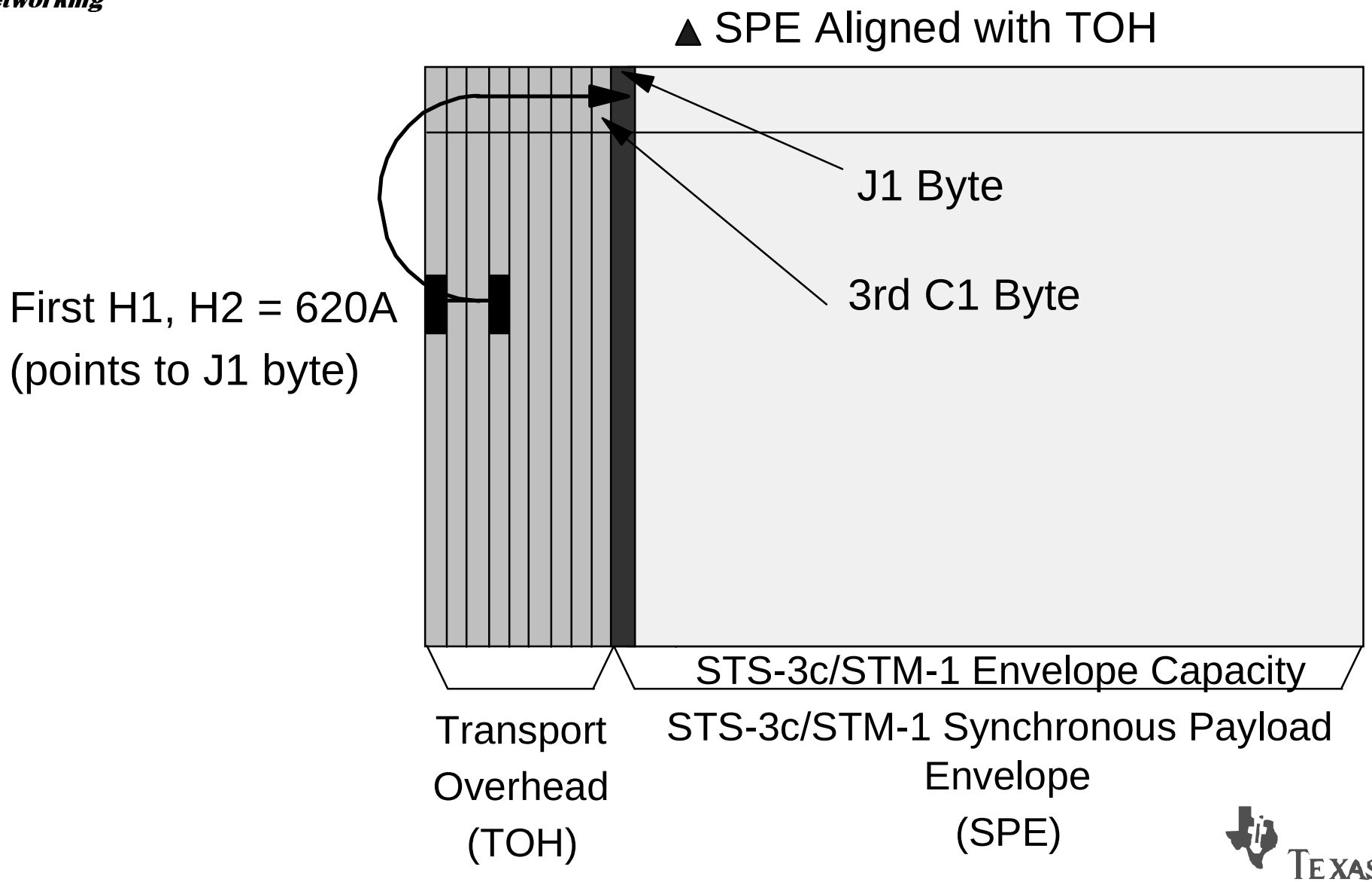
Driving ATM Into Mainstream Networking

SONET/SDH Frame Processing



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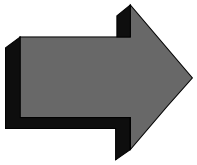
SONET/SDH as a Physical Layer for ATM

- Standards bodies and standard rates
- The four layers of SONET/SDH
- Terminating equipment
- Frame structure
- Overhead bytes
- SONET/SDH mapping for ATM
- Differences between SONET and SDH



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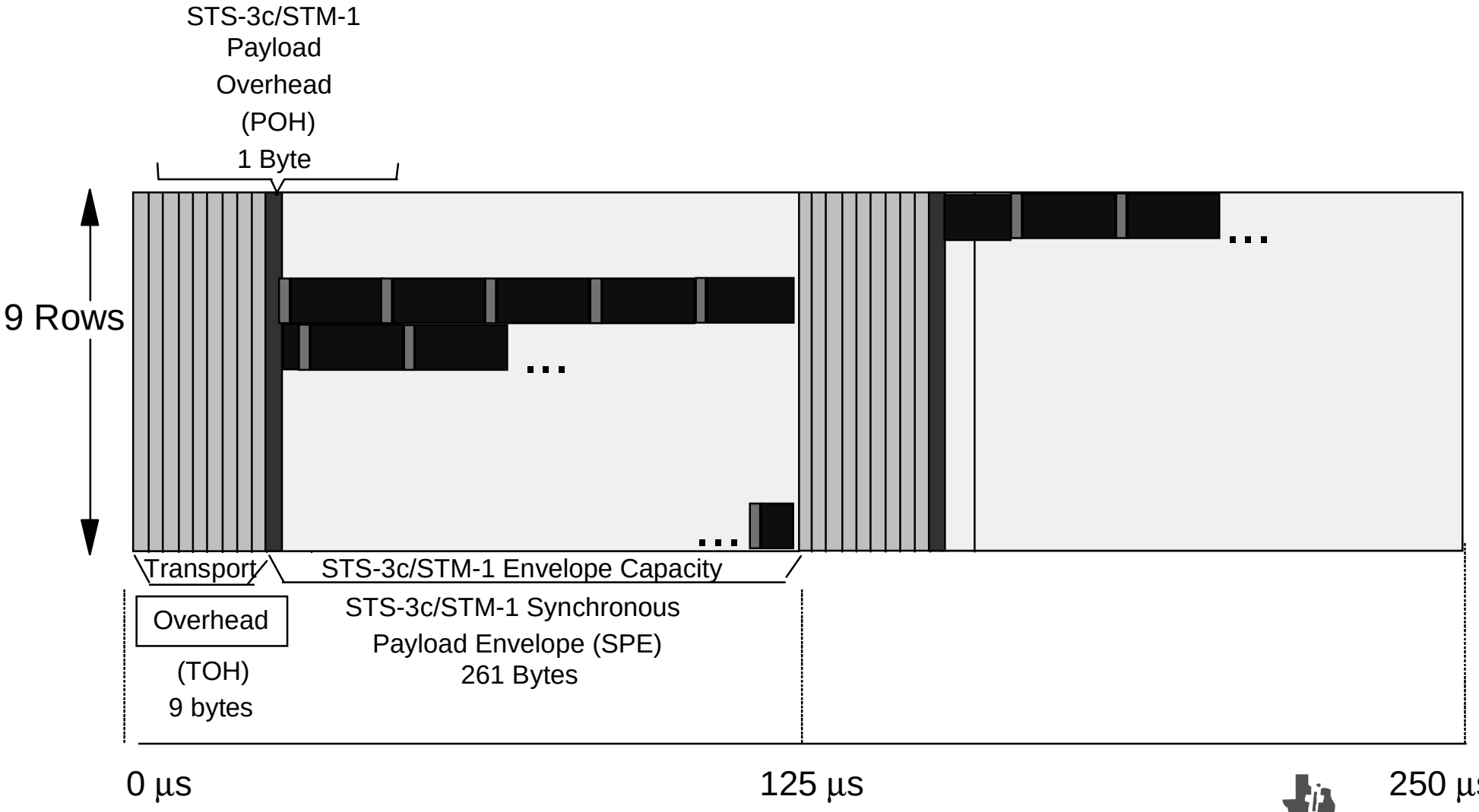
MAPPING AN ATM CELL INTO A SONET/SDH FRAME



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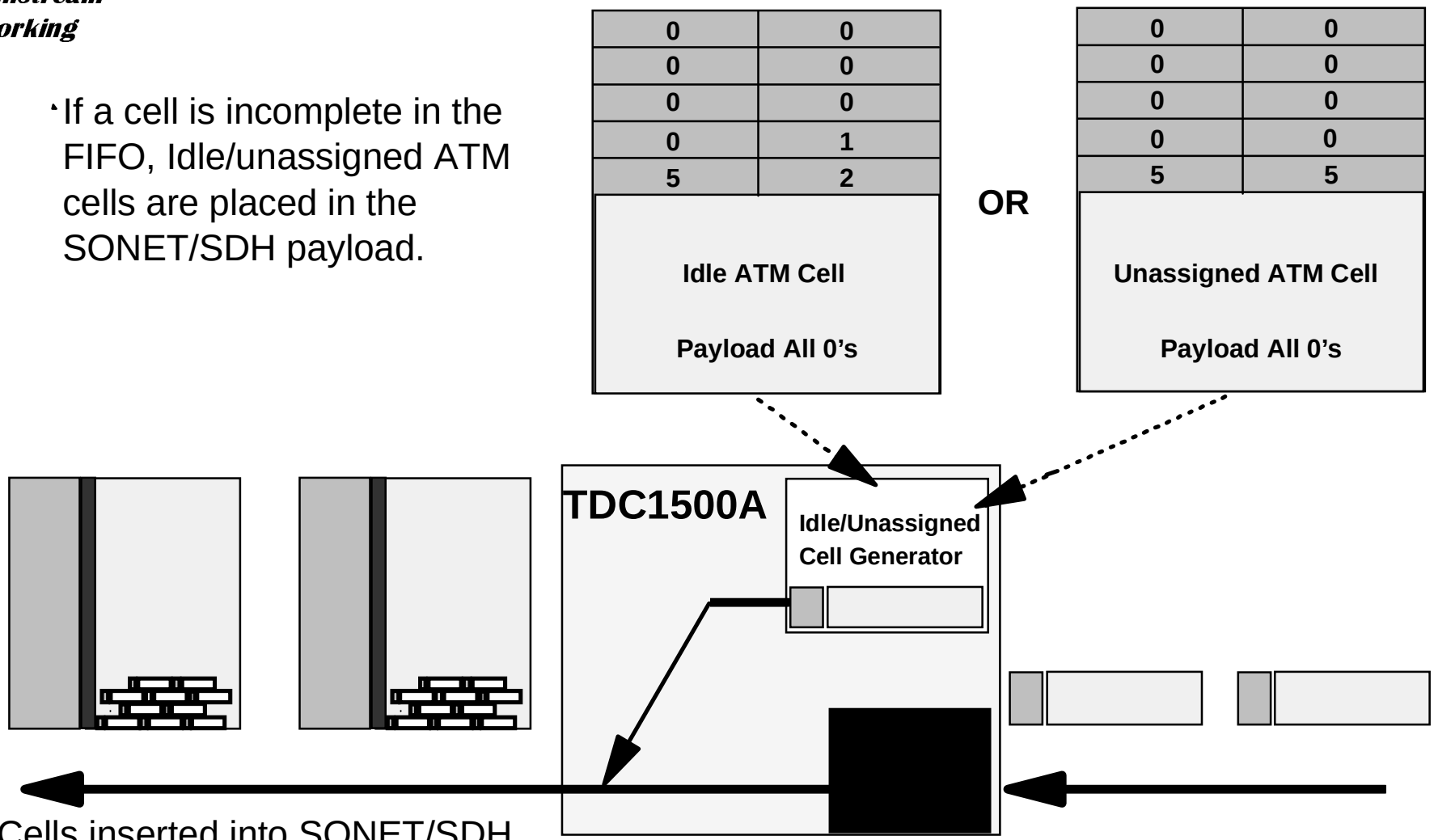
Transmit Data Flow

- If a cell is incomplete in the FIFO, Idle/unassigned ATM cells are placed in the SONET/SDH payload.



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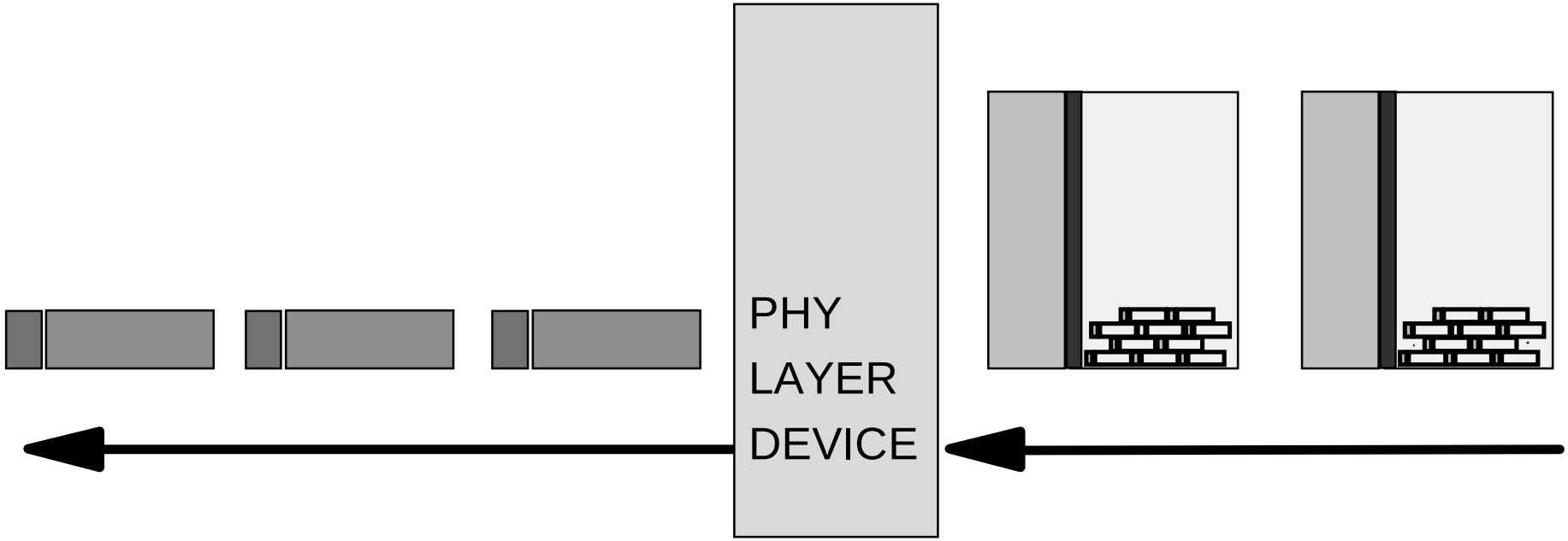
Receive Data Flow



ATM cells passed to SAR device

- Cell header
- Cell payload

SONET/SDH frames received from physical media device

- Transport overhead
- Path overhead
- Payload envelope

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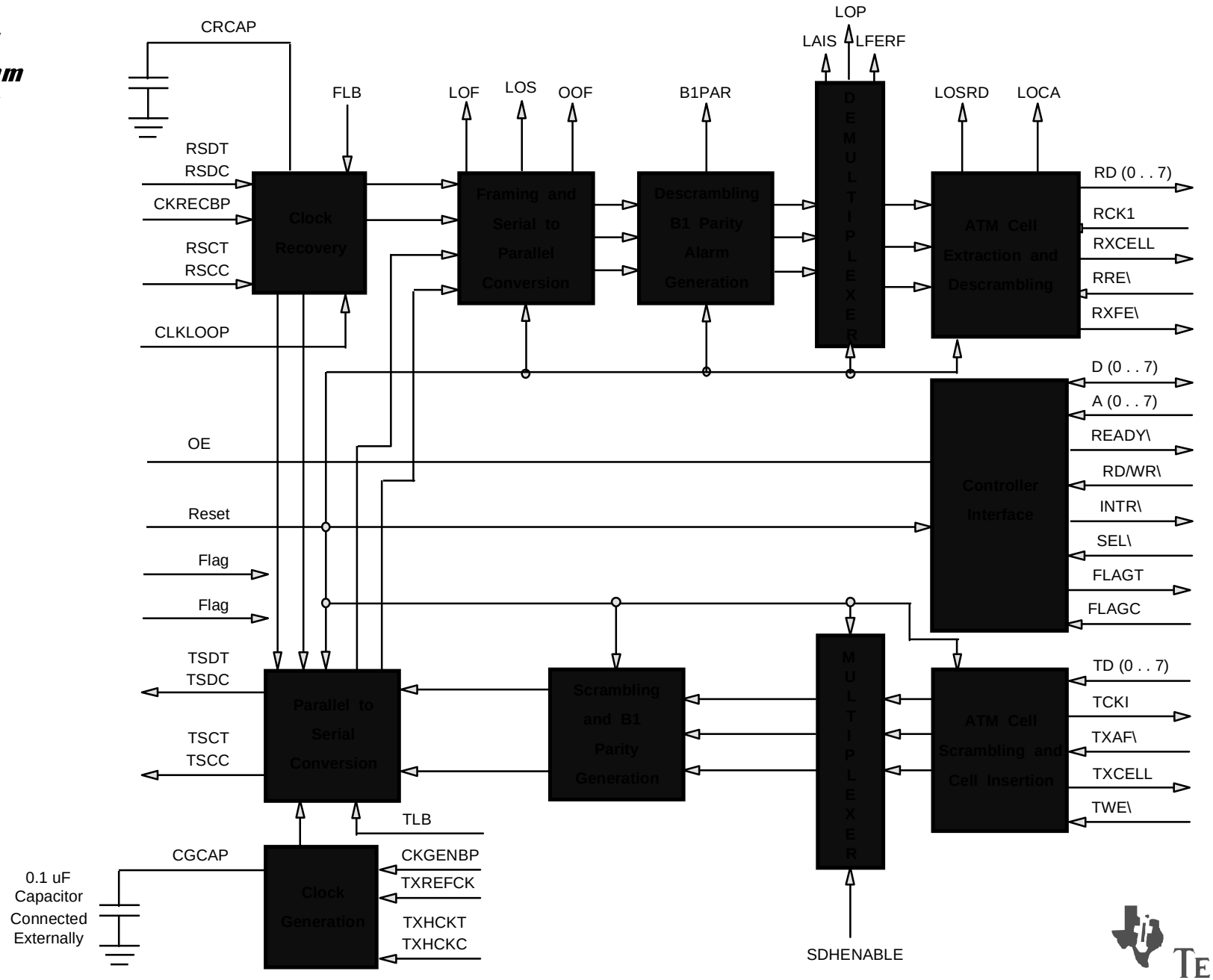
SABRE Architecture



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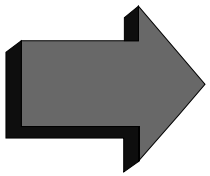

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Differences Between SONET and SDH

	SONET	SDH
1st C1 Byte	0000 0001	0000 0001
2nd C1 Byte	0000 0010	0000 0000
3rd C1 Byte	0000 0011	0000 0000
1st H1 pointer Byte	0110 0010	0110 1010
2nd H1 pointer Byte	1001 0011	1001 1011
3rd H1 pointer Byte	1001 0011	1001 1011

Differences Between Idle Cells and Unassigned Cells

Idle Cell	Header = 00 00 00 01 52
Unassigned Cell	Header = 00 00 00 00 55

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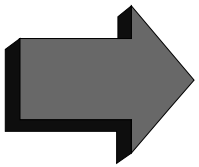
SONET/SDH and ATM The Local Area Network Agenda



- Section 1: Physical layers for ATM*
- Section 2: SONET**/SDH*** as a physical layer for ATM
- Section 3: ATM
- Section 4: ATM and related protocols
- Section 5: TI™ solutions

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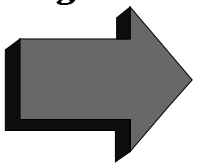
Asynchronous Transfer Mode



- ATM overview
- ATM cell structure
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- Virtual channels and virtual paths
- Key differences between ATM and 802.x
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  - Interleaved cells vs packet bursts
  - Cells routed in order
  - VPI/VCI usage

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ATM FORUM

Charter

"To accelerate the use of ATM products and services through rapid convergence and demonstration of interoperability specifications, and promotion of industry cooperation and awareness"

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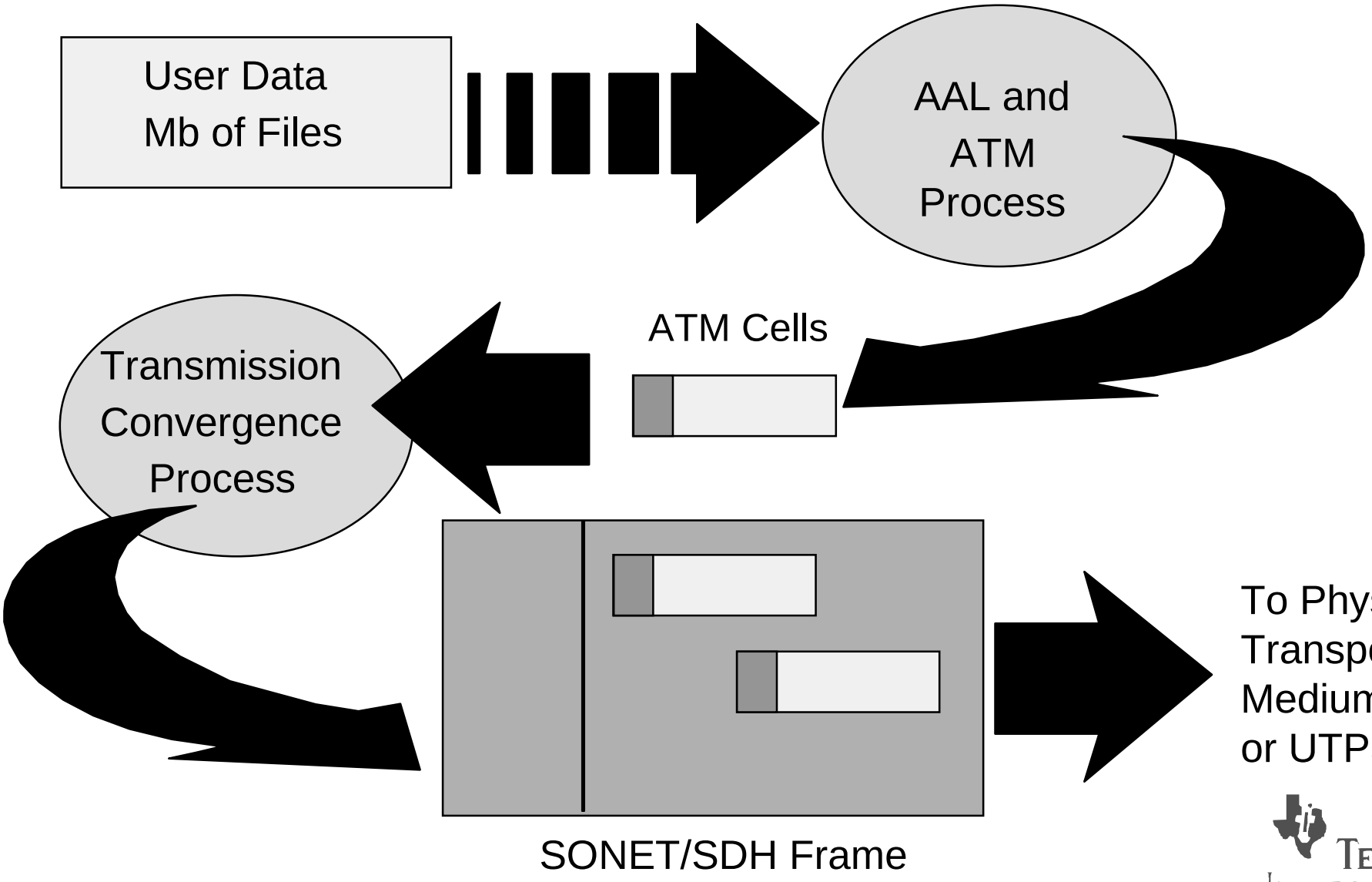
THE ATM COMMUNICATION PROCESS



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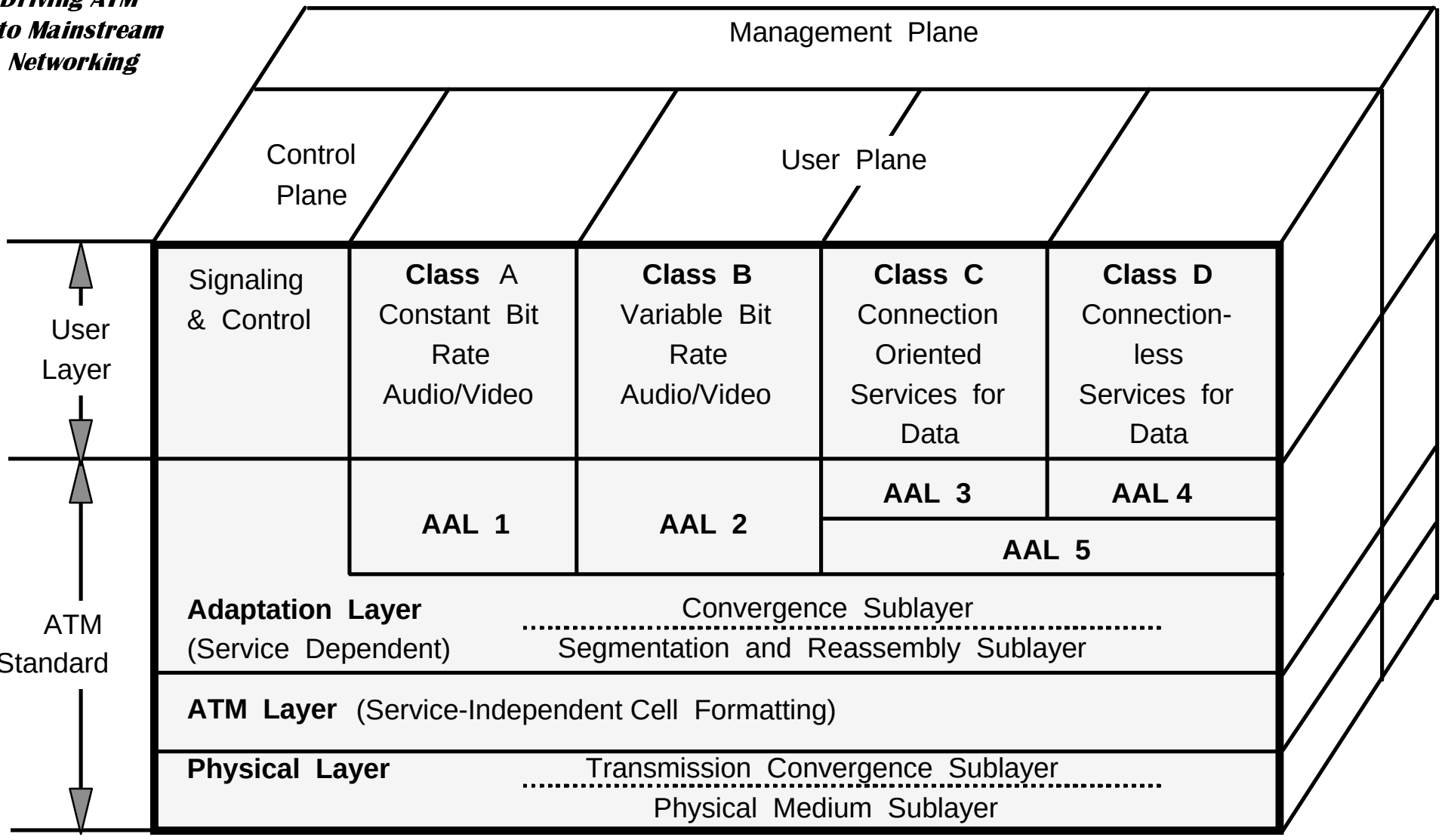
B - ISDN REFERENCE MODEL



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FUNCTIONS OF THE ATM LAYERS

LAYER MANAGEMENT	HIGHER LAYER FUNCTIONS	HIGHER LAYER	
	Convergence Sublayer	CS	AAL
	Segmentation and Reassembly	SAR	AAL
	Generic Flow Control Cell Header Generation / Extraction Cell VPI / VCI Translation Cell Multiplex and Demultiplex	ATM	
	Cell Rate Decoupling HEC Sequence Generation / Verification Cell Delineation Transmission Frame Adaption Transmission Frame Generation / Recovery	TC	Physical Layer
	Bit Timing Physical -Medium Dependent	PMD	Physical Layer

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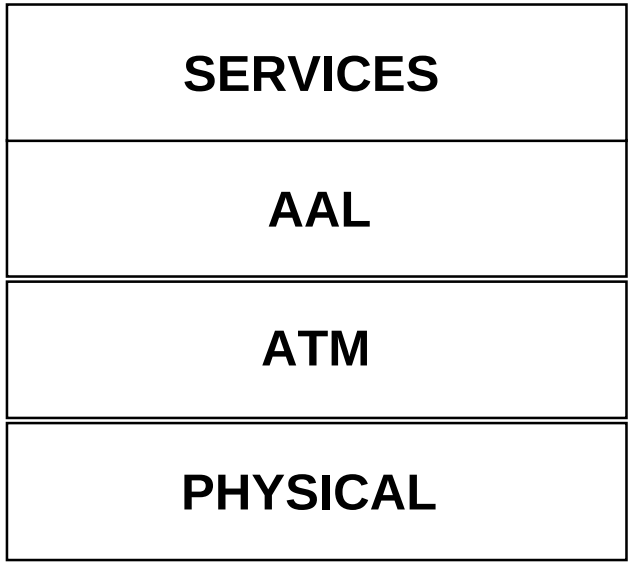
LAYERED PROTOCOL STACK MODEL

The means to implement the transmission of datagrams across the network is done according to protocol rules established at separate layers.

This simplifies peer-to-peer communications between layers.



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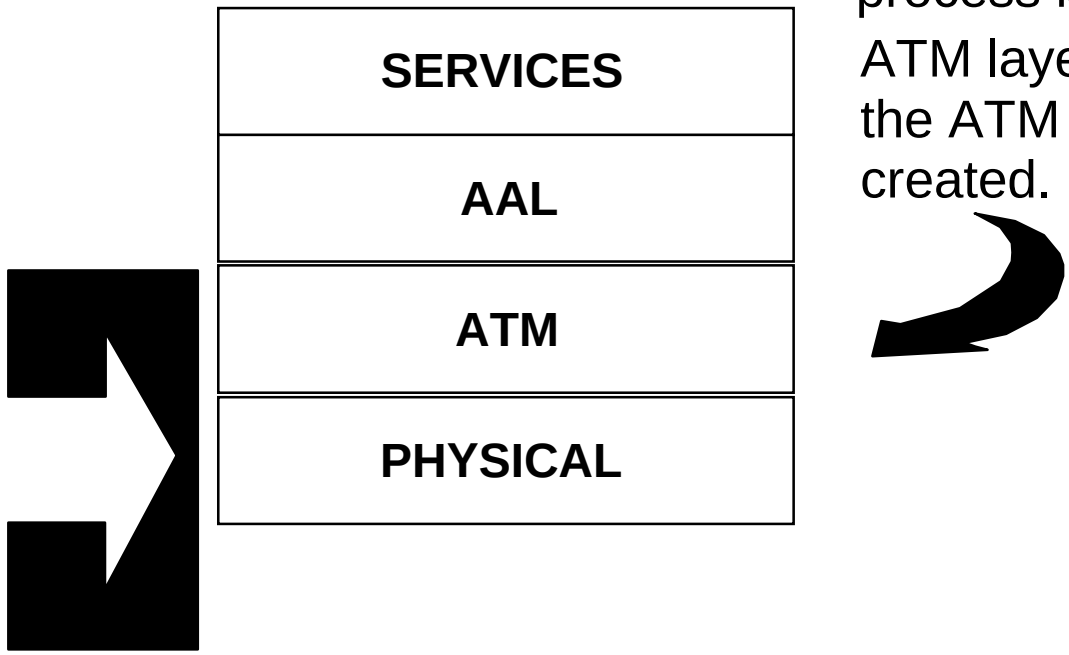
FUNCTIONS OF THE DIFFERENT LAYERS

The heart of the process is in the ATM layer, where the ATM cell is created.



The bottom three layers define the ATM communications process.

Each of the sublayers has unique layer responsibilities for the decoding of serial information to higher-layer protocol data units

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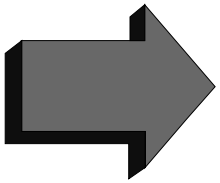
Asynchronous Transfer Mode



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Driving ATM Into Mainstream Networking

THE ATM UNI AND NNI CELL HEADER

- **Two major types of ATM interfaces defined**
  - **User-to-network interface (UNI)**
  - **Network-to-network interface (NNI) (also referred to as network-to-node interface)**
- **UNI interface used by client node to access ATM switch**
- **NNI interface is used by switching fabric to communicate to other ATM switches. VPI field is larger to accommodate greater use of virtual paths at network layer.**

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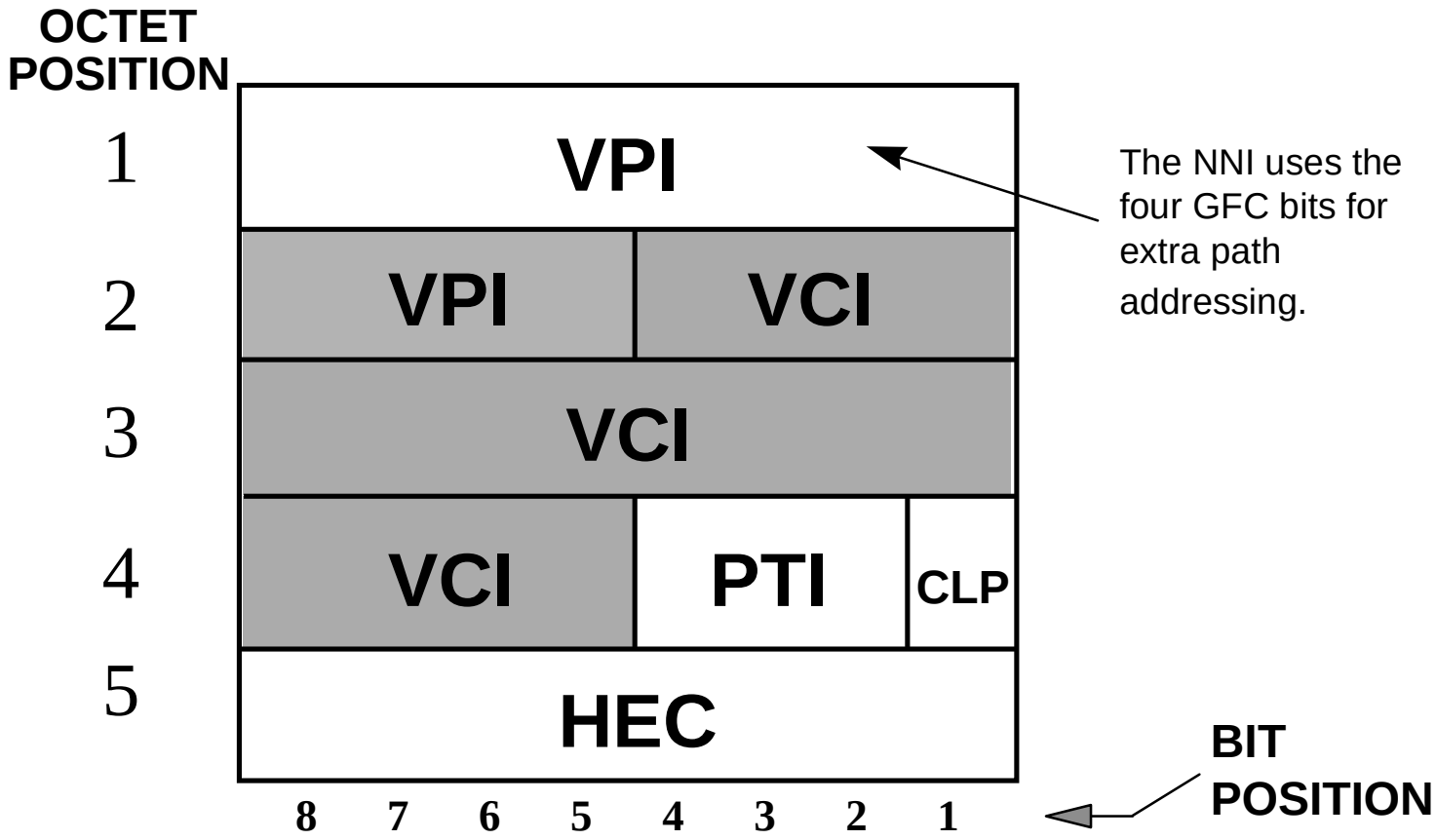
THE ATM NNI CELL HEADER



VPI= Virtual Path Identifier
VCI= Virtual Channel Identifier
PTI= Payload Type Indicator
CLP= Cell Loss Priority
HEC= Header Error Control
NNI= Network-to-Network Interface

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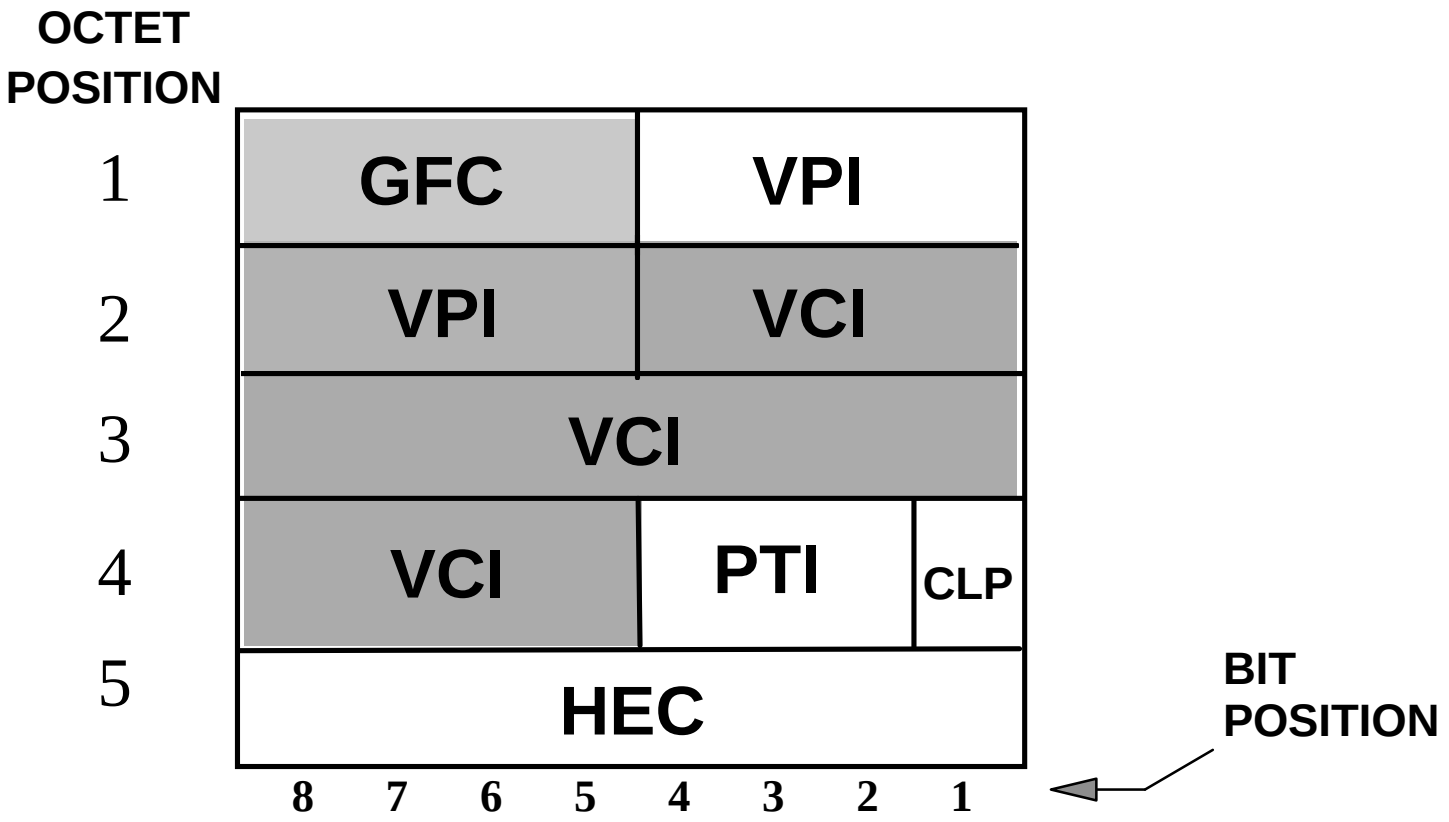
THE ATM UNI CELL HEADER



VCI= Virtual Channel Identifier

GFC= Generic Flow Controller

-undefined and usage controversial

CLP= Cell Loss Priority

- discard cells preferentially

UNI= User-to-Network Interface

VPI= Virtual Path Identifier

HEC= Header Error Control

PTI= Payload Type Indicator

- Bit 3: Discrim. between data and op. cells
- Bit 2: Indicates congestion upstream
- Bit 1: User indication (set for last cell with AAL5)

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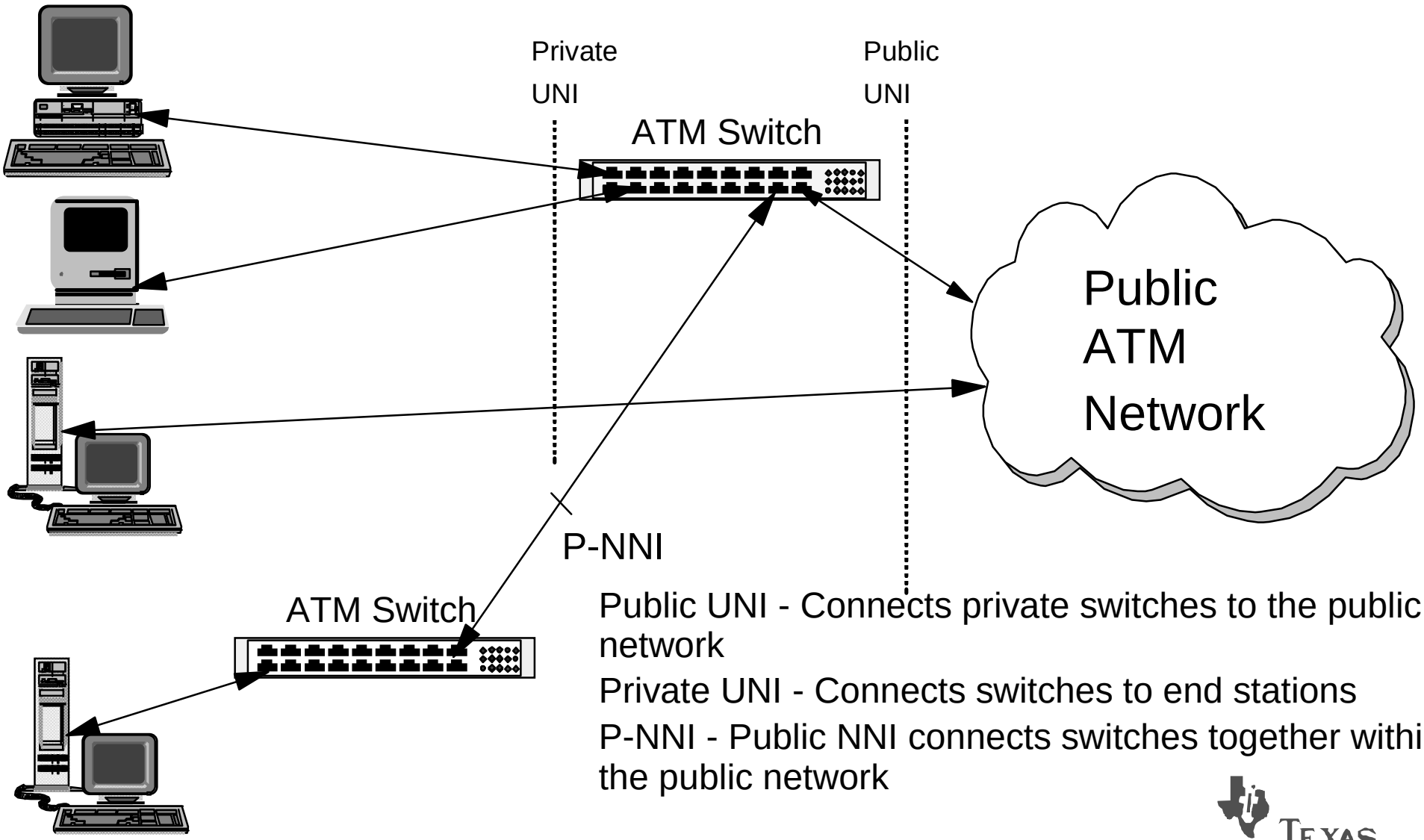
UNI AND NNI NETWORK INTERFACES



Public UNI - Connects private switches to the public network

Private UNI - Connects switches to end stations

P-NNI - Public NNI connects switches together within the public network

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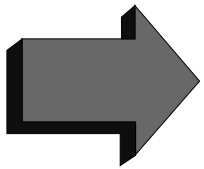
Asynchronous Transfer Mode



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- Implementation block diagrams

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SERVICE DEMAND ON NETWORK LATENCY AND BANDWIDTH

Services	Telephone	Data	Cable TV	Video Conferencing
Parameters	Connection Oriented	Connectionless	Connections	Connection Oriented
	Delay Variance Sensitive	Delay Variance Insensitve	Delay Variance Insensitive	Delay Variance Sensitve
	Lag Sensitive	Lag Insensitive	Lag Sensitive	Lag Sensitive
	Low Bandwidth	High Bandwidth	High Bandwidth	High Bandwidth
	CBR	VBR	CBR	CBR & VBR

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THE ATM ADAPTATION LAYER

The AAL process is the most important feature of the ATM communications process.

How the adaptation process is carried out depends on the type of service to be transported.

AAL Type	Service Type	Comments
AAL1	Constant Bit Rate (CBR)	Isochronous traffic like DS0, DS1s, DS3s to permit voice
AAL2	Variable Bit Rate (VBR)	For data services (Packet Video?) AAL for i/f w/ Video Codecs, etc.
AAL3	Connection-Oriented VBR Data Transfer	For bursty data over long period
AAL4	Connectionless VBR Data Transfer	For short bursty data (SMDS)
AAL5	Simplified AAL	Mainly for point-to-point

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CLASSES OF ATM SERVICE

	Class A	Class B	Class C	Class D
Timing Relation Between Source and Destination	Required		Not Required	
Bit Rate	Constant	Variable		
Connection Mode	Connection Oriented			Connectionless
AAL Types	1	2	3/4, 5	3/4

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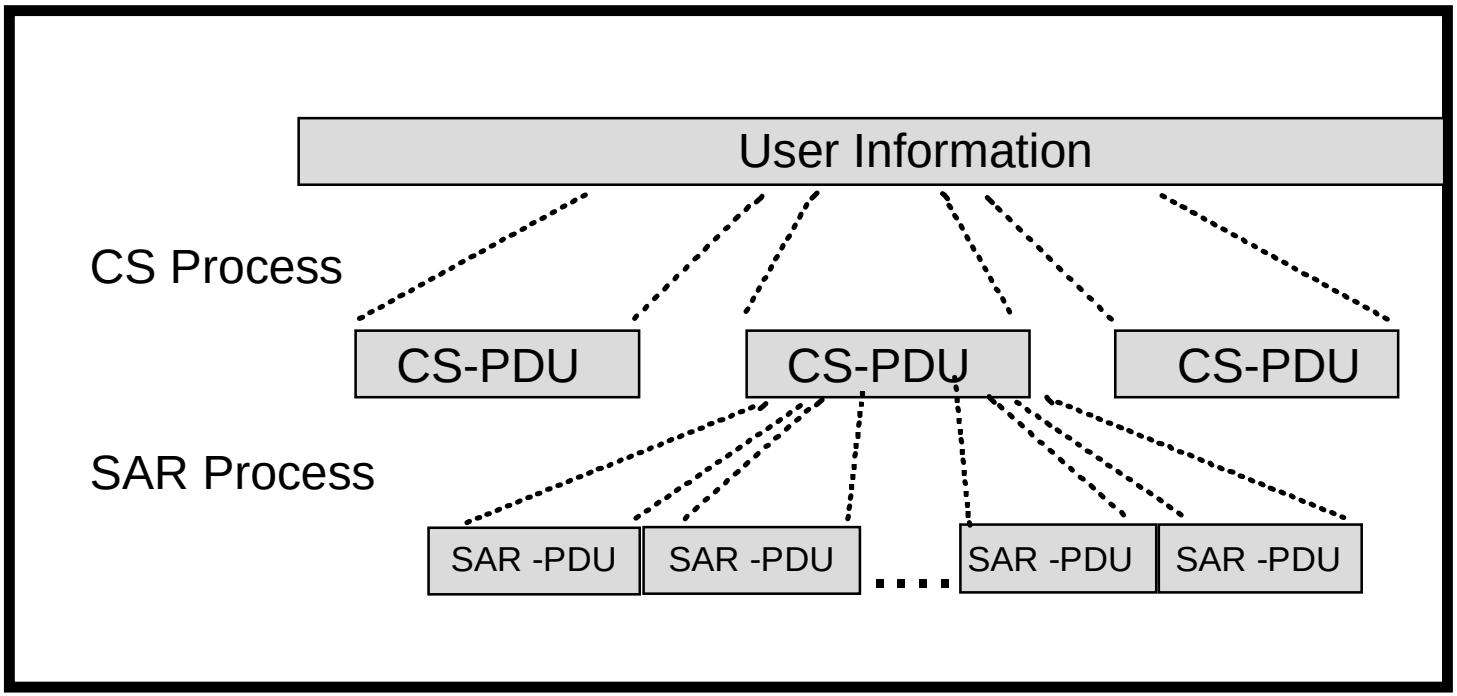
THE AAL PROCESS

AAL is divided into two sublayers.

Convergence Sublayer

and

Segmentation and Reassembly Sublayer.



These two sublayers convert the user information into 48-byte cell payloads. Each sublayer produces a protocol data unit (PDU). The CS-PDU is variable length while the SAR-PDU is always 48 bytes.

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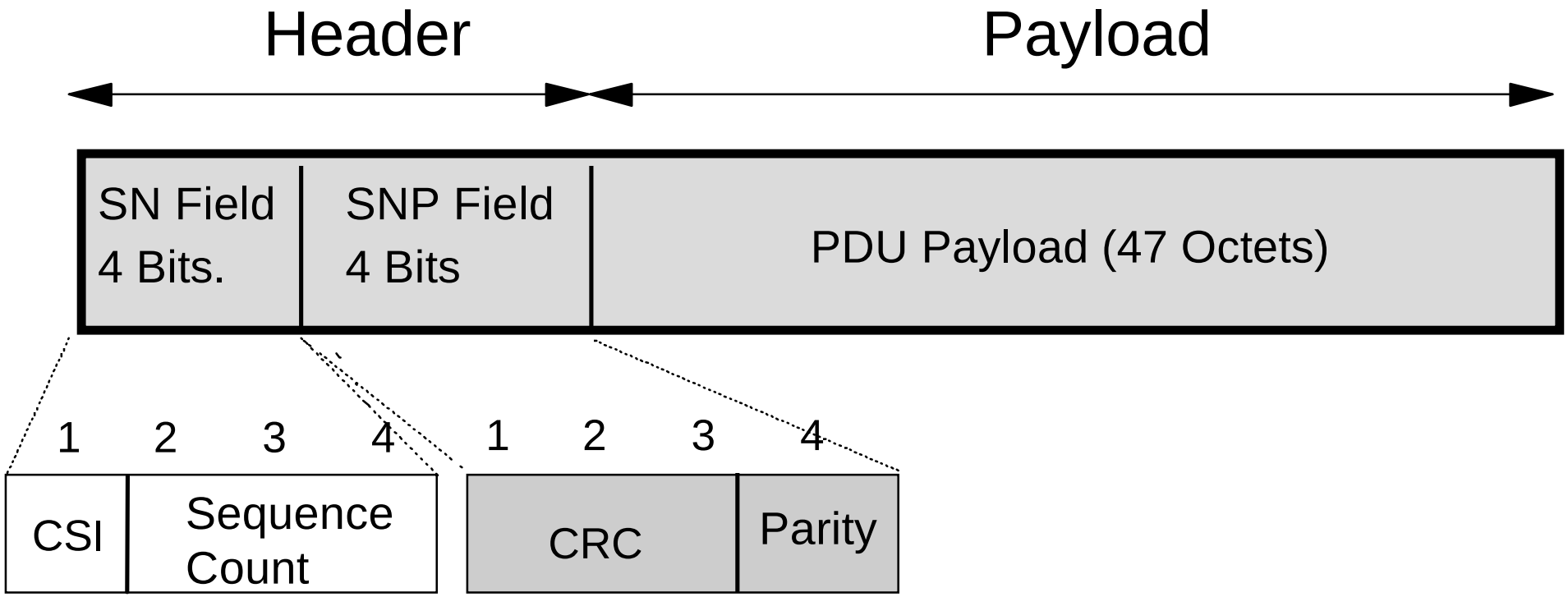
AAL1 Processing



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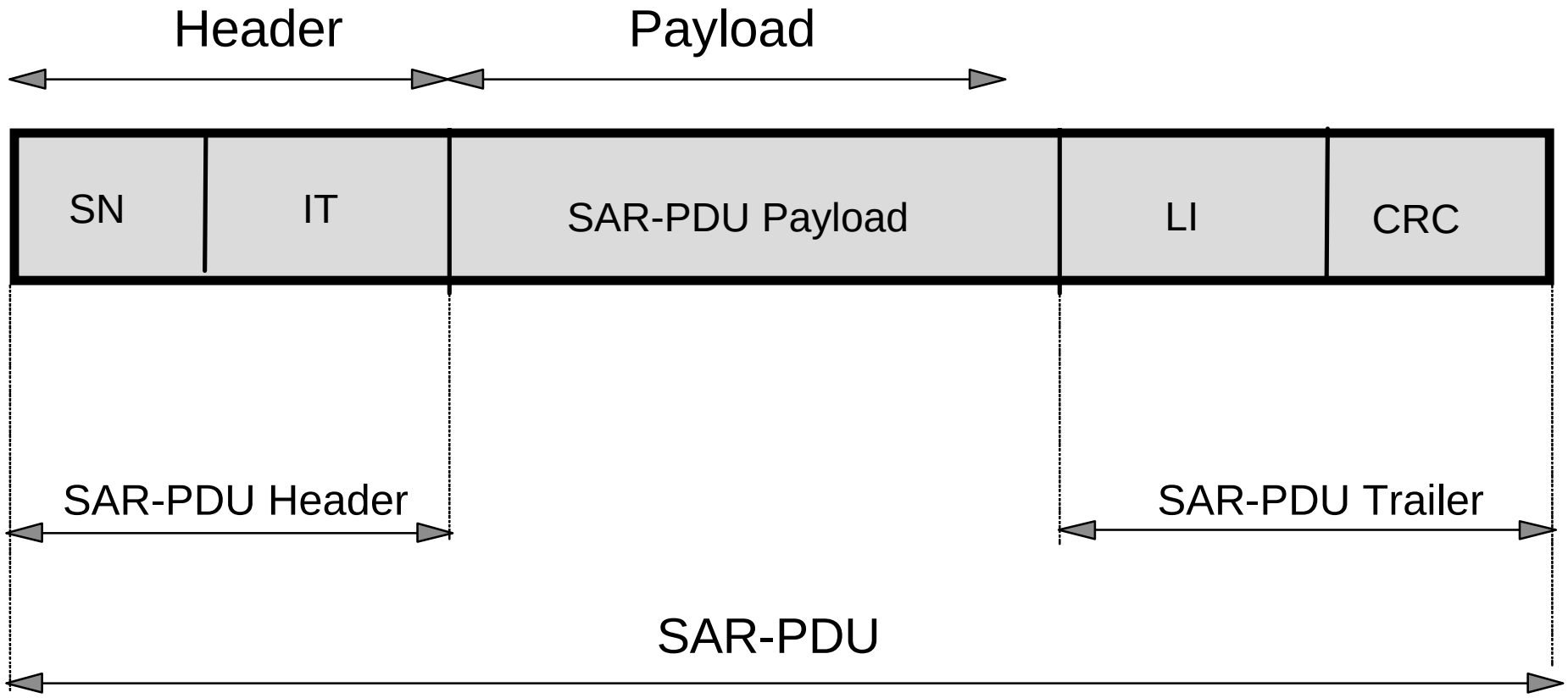
AAL2 Processing



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THE AAL PROCESS: AAL3/4 CS-PDU

CPI	Common point indicator
BTag	Beginning tag (1 byte)
BA Size	Buffer allocation size (2 bytes)
Info Payload	Length of payload (max 65,535 bytes)
Pad	Up to 3 bytes – used to align CS-PDU length
AL	Alignment (1 byte)
ETag	End tag (1 byte)

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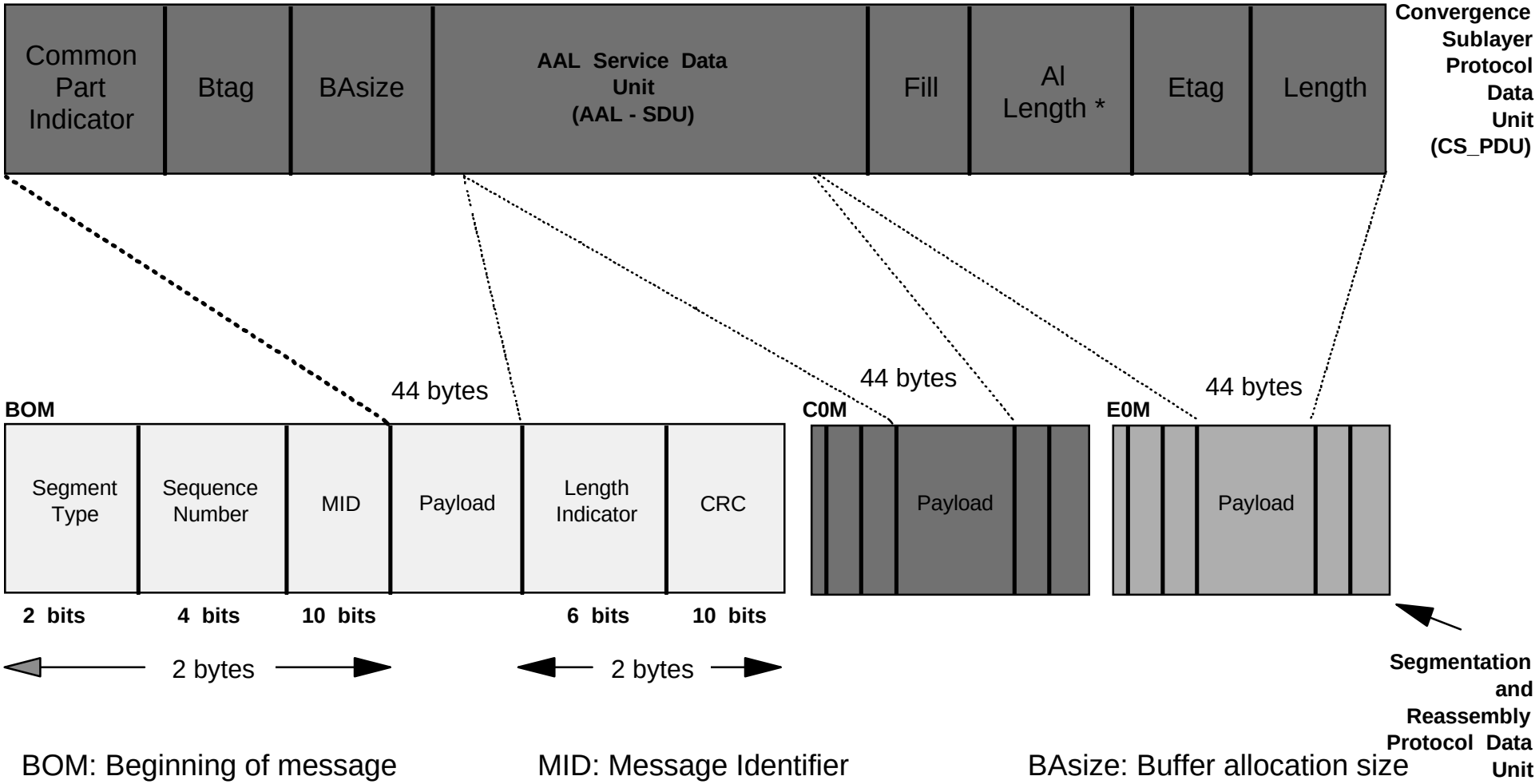
AAL3/4



BOM: Beginning of message
COM: Continuation of message
EOM: End of message

MID: Message Identifier
CRC: Cyclic Redundancy Check
EOM: End of message

BAsize: Buffer allocation size
Btag: Beginning tag
Etag: End tag

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THE AAL PROCESS: AAL5 CS-PDU

Information Payload	Maximum length of 65 535 bytes
Pad	Maximum of 47 bytes used to align the CS-PDU length to a multiple of 48 bytes
Control	Used to transfer user-to-user information
Length	Indicates the length of the information payload
CRC-32	32-bit CRC that is computed across the entire information payload

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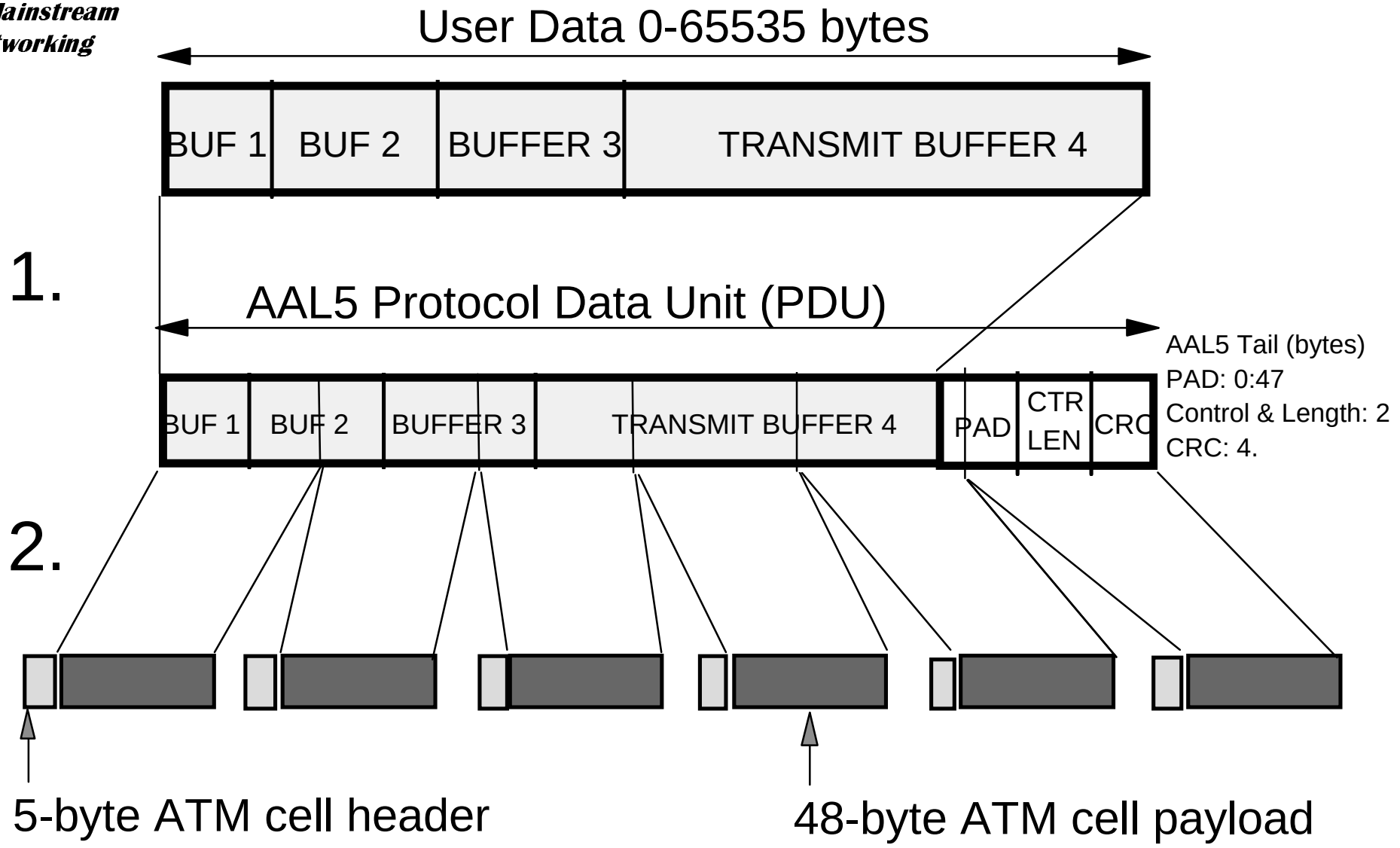
AAL5



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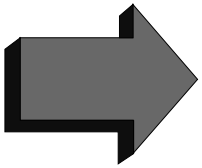
Driving ATM Into Mainstream Networking

Asynchronous Transfer Mode



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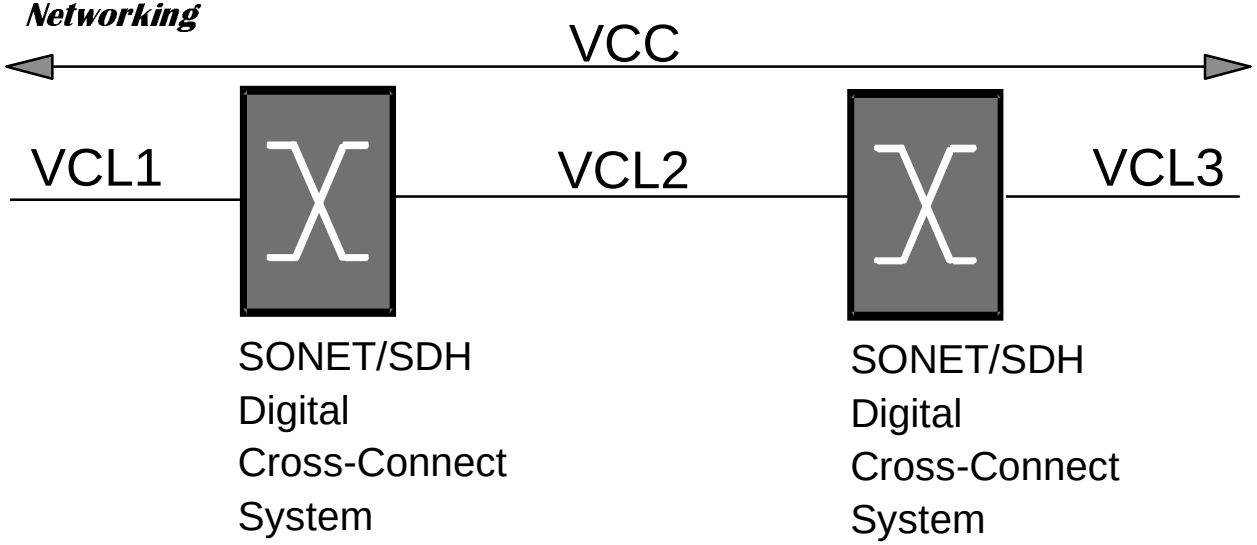
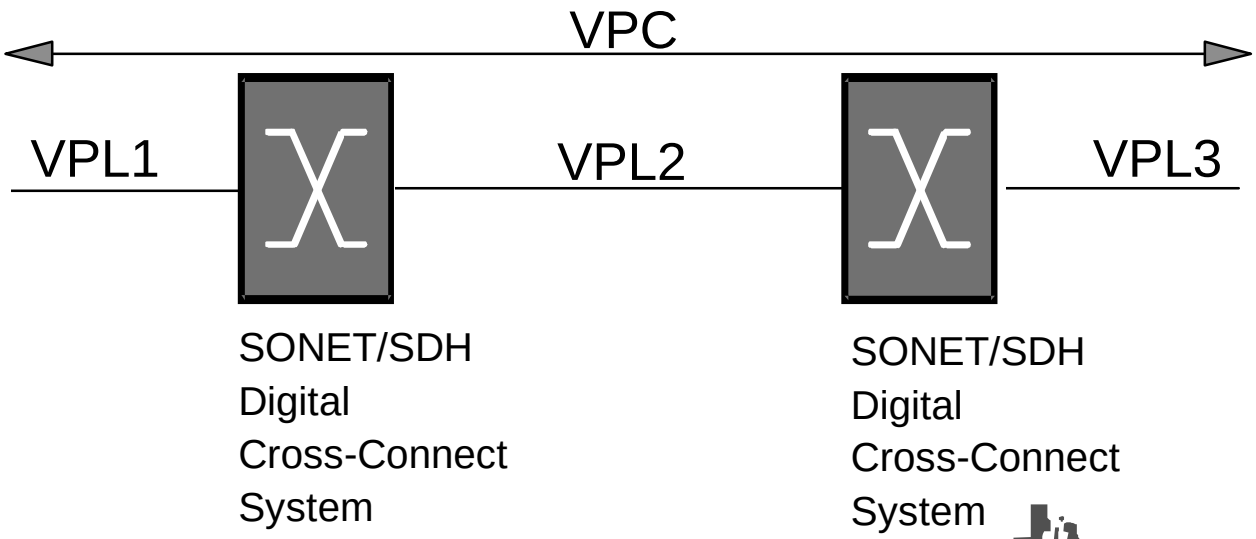
VCL/VPL and VCC/VPC



Typically, UNI operates in VCI mode, which means that virtual circuits are identified by a VCI value alone, with the VPI field being set to a default value for all circuits across the UNI.

In VPI operation, a number of virtual circuits are allocated different VCI values, but the same VPI value. Intermediate switches then switch all cells with the same VPI value between the same links, ignoring (and not changing) the VCI values.



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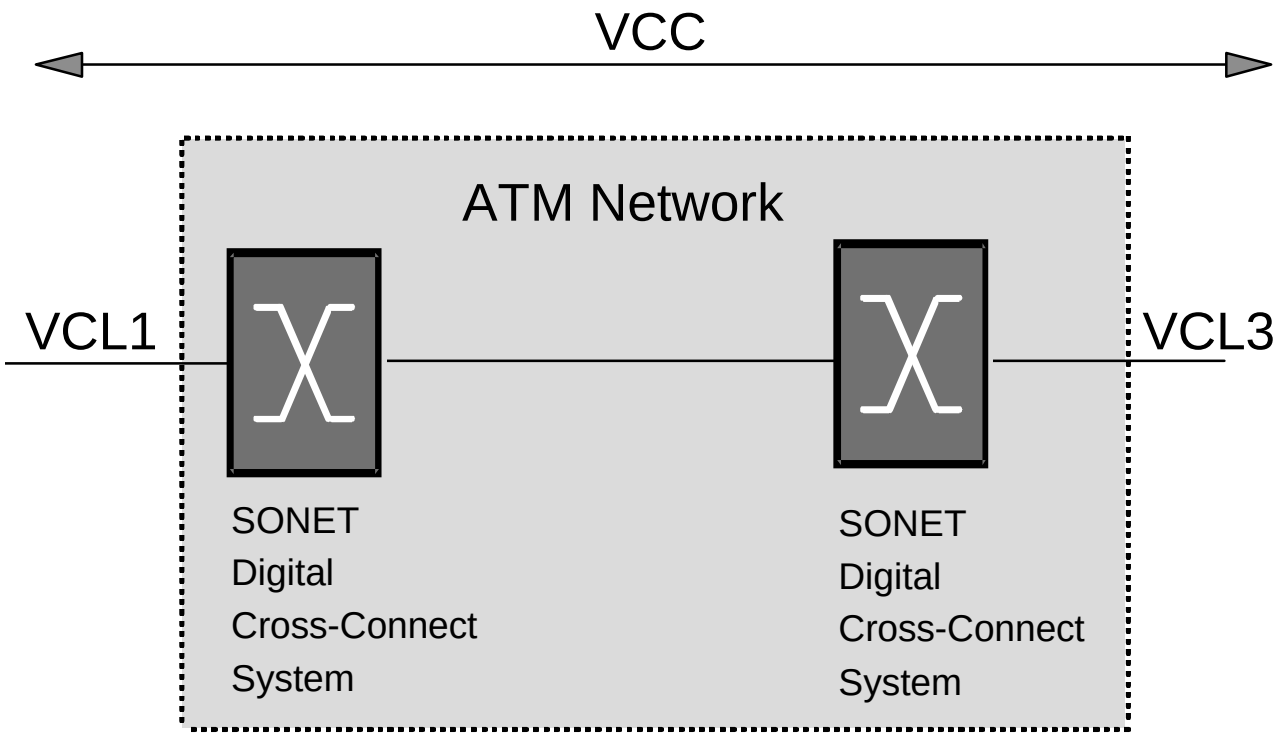
VCL/VPL and VCC/VPC



Note that for management purposes, an ATM network can be viewed as a large distributed switch by hiding all the network's internal connectivity, as if internal to the distributed switch. This model, for example, may be used for customer network management (CNM) purposes.

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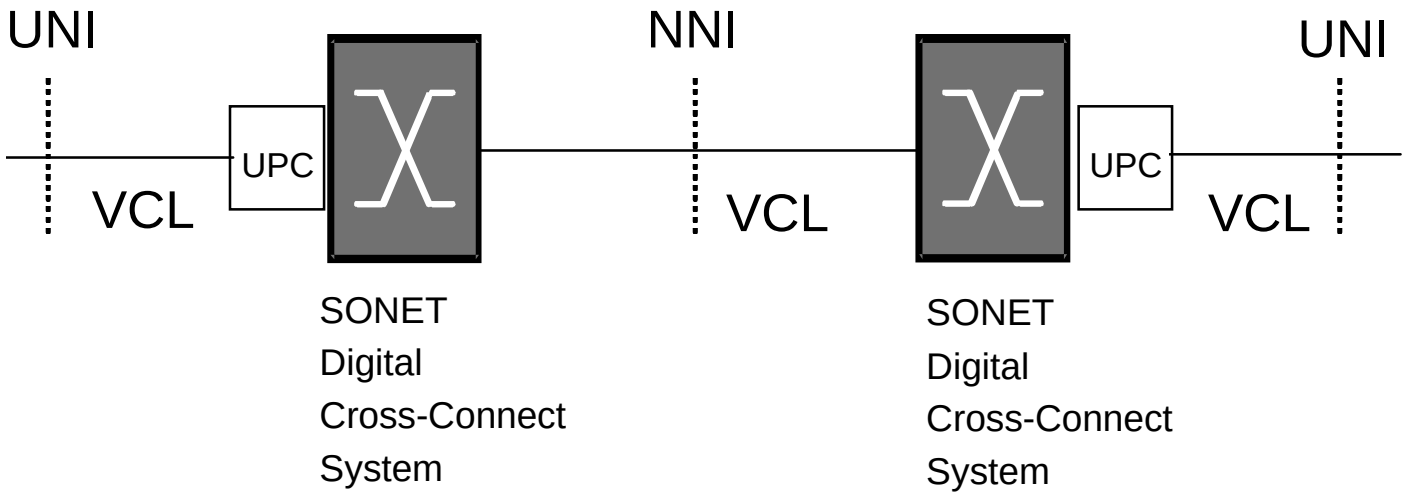
Traffic Shaping Parameters



The traffic enforcement or policing action taken at the UNI is called usage parameter control (UPC) and is activated on an incoming VCL or VPL.

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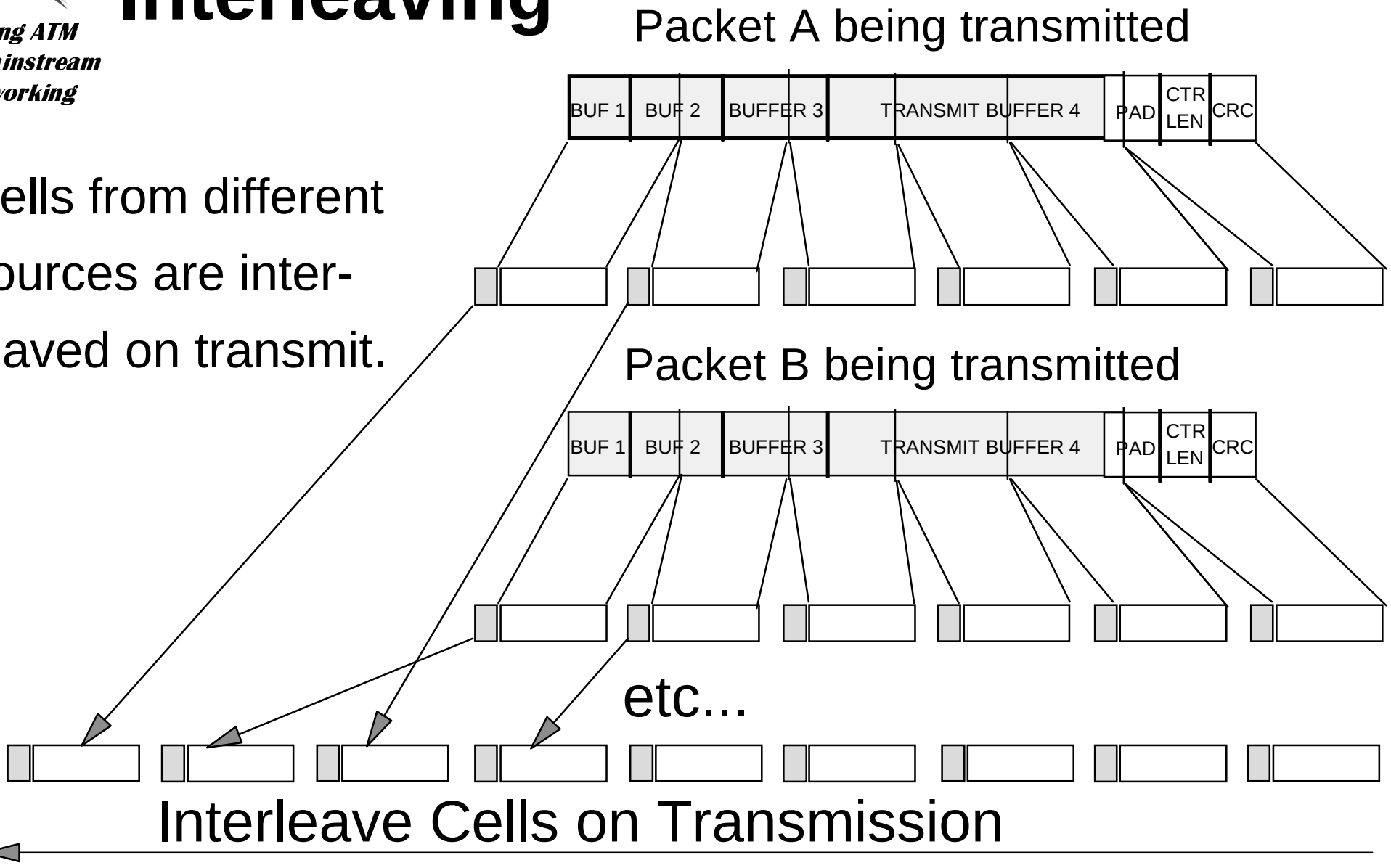
Interleaving

Cells from different sources are inter-leaved on transmit.



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Interleaved Cells vs Packet Bursts

- LAN packets vary in length, from 17 to >4500 bytes, requiring memory/processing power.
- LAN packets must be transmitted contiguously for the entire length of the packet without break.
- ATM has fixed packet lengths; payload and header are always in the same place.
- ATM cells are uniform in size, and, therefore, more manageable in hardware implementations.

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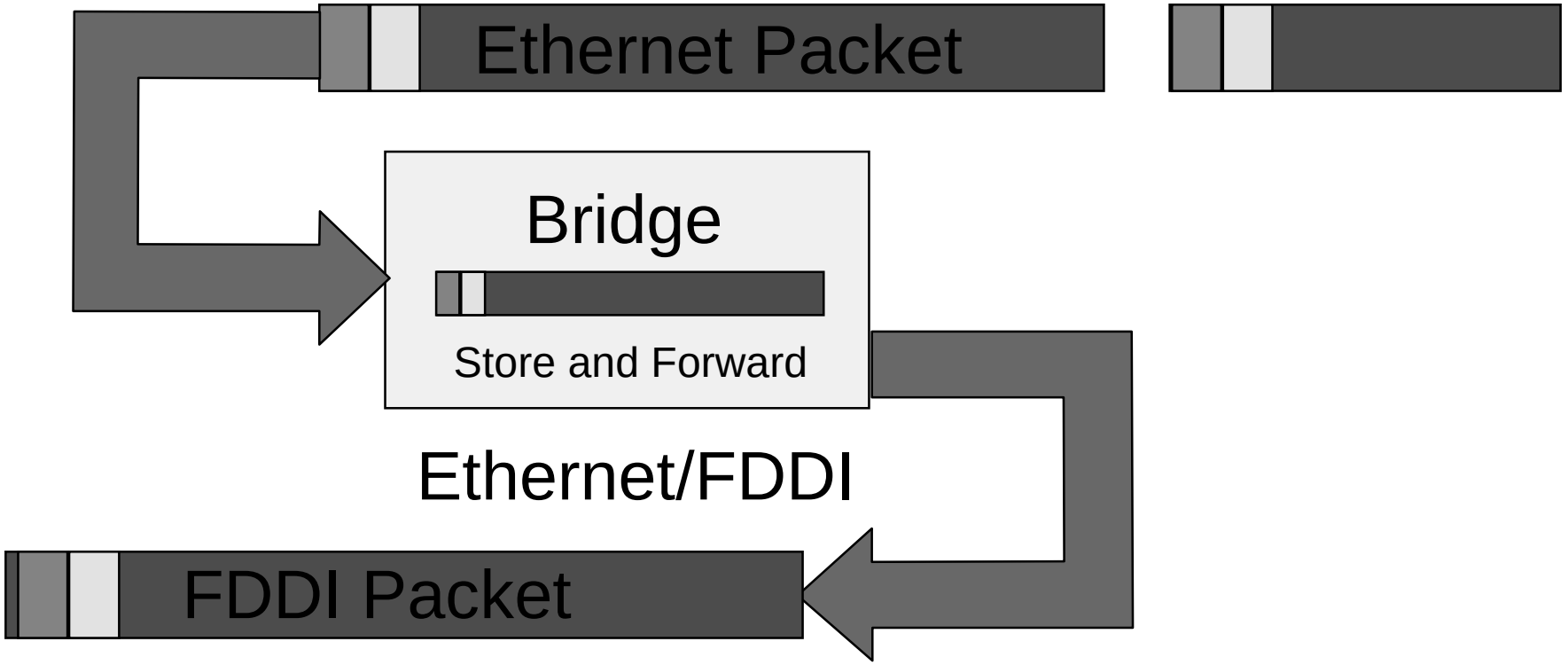
Benefits of Interleaving



- An Ethernet packet cannot be forwarded immediately after it is received to FDDI.
- Hence, latencies can be large, especially for multiport bridges.

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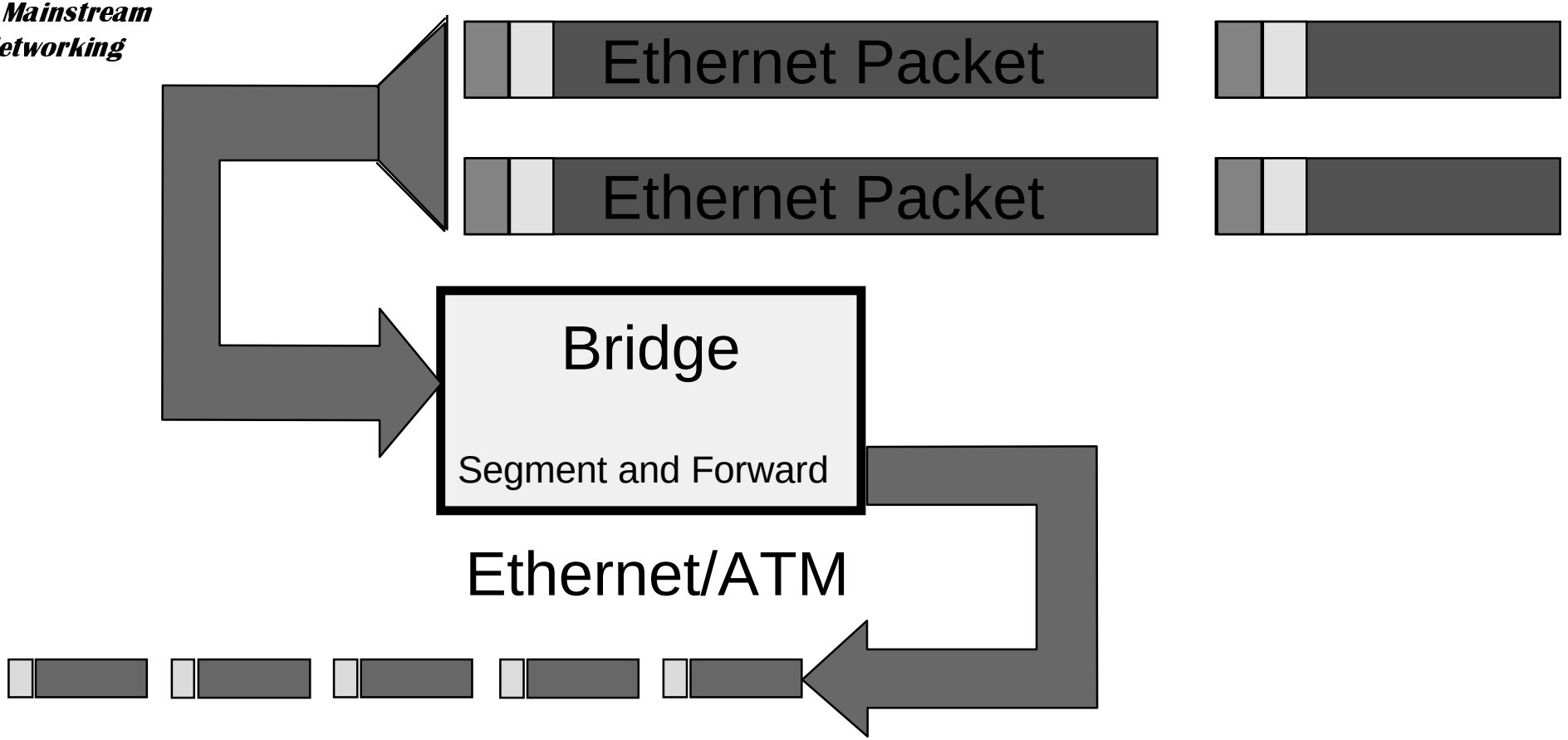
Benefits of interleaving



- An Ethernet packet, as soon as it is received, can be segmented and forwarded to ATM.
- Hence, latencies can be minimized, especially for multiport bridges.

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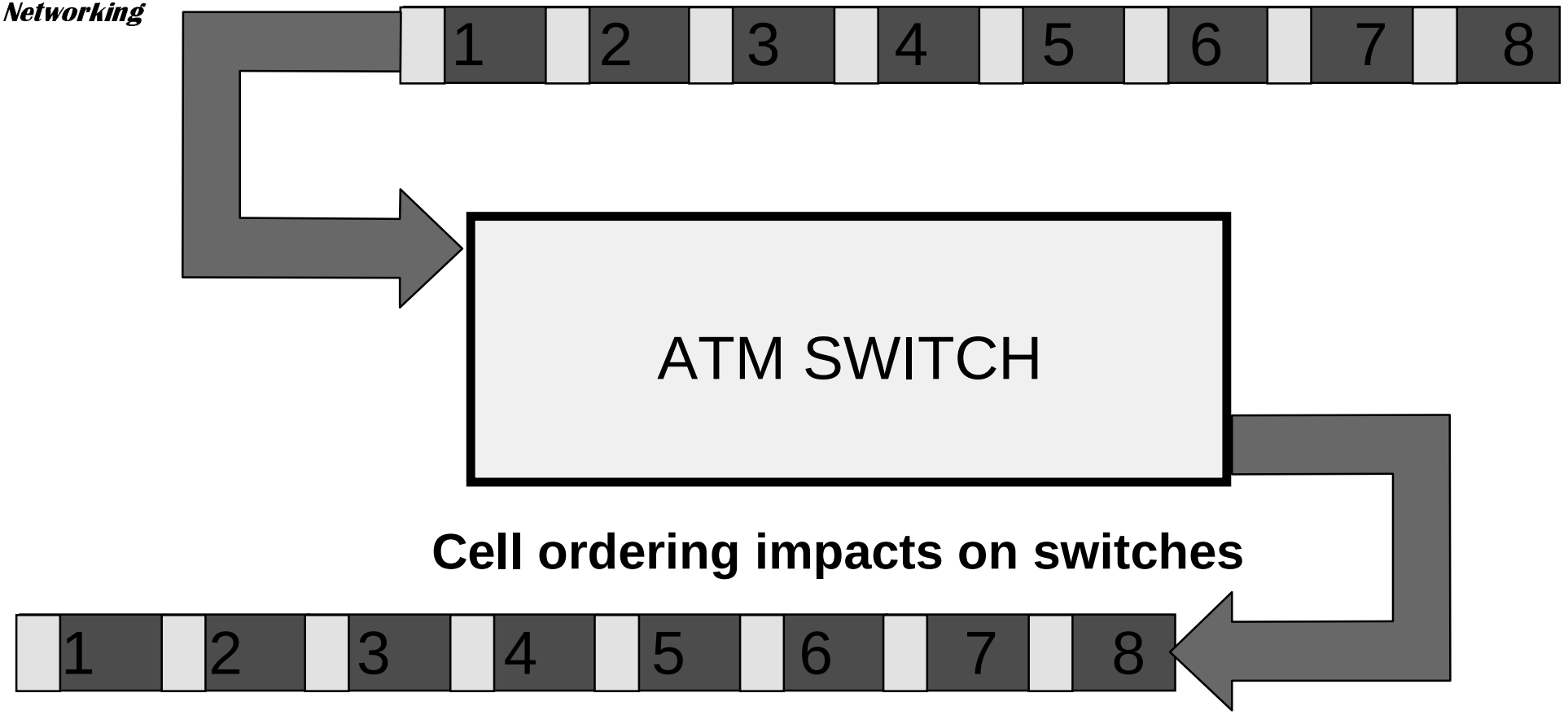
Cells Routed in Order



Cell ordering impacts on switches

Switches have to ensure that the cells are transmitted in the order of reception. Implementation complexity depends on the switch architecture.

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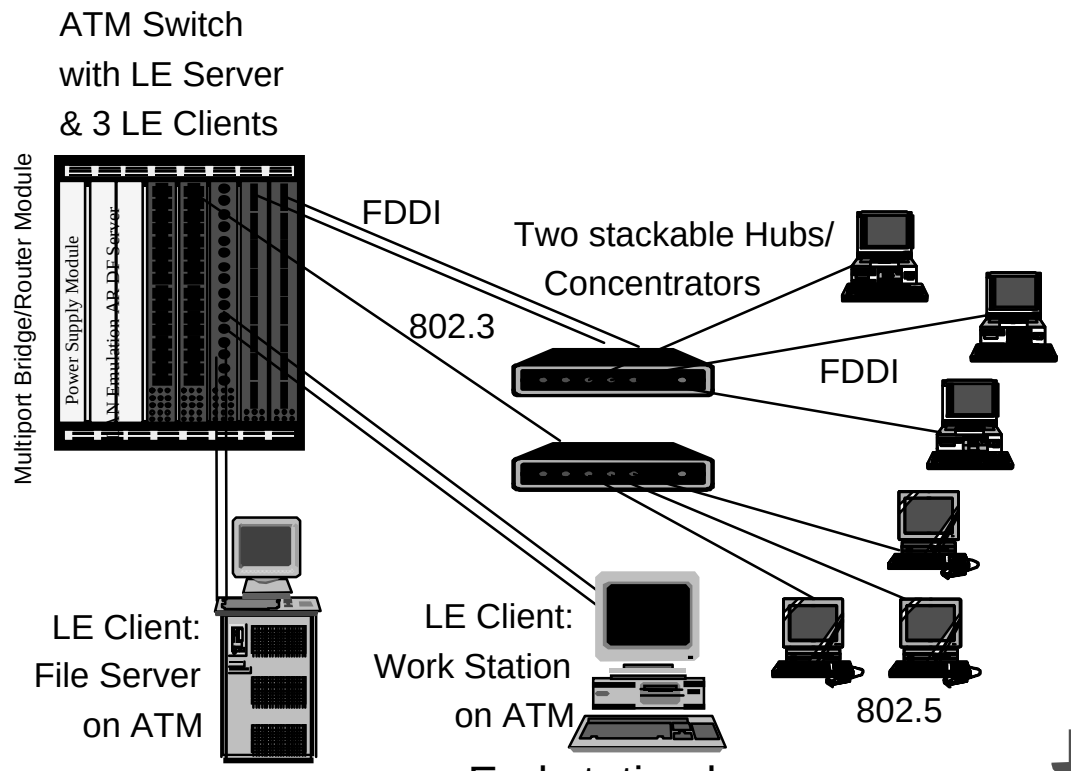
VPI/VCI Usage

- End stations tend to require processing on only a few VPI/VCIs.
- Switches and hubs that process a large number of connections need to process more VPI/VCIs.

Switch has many connections open.



End station has just a few VPI/VCI

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VPI/VCI Impacts on Receive Engine

- **We have seen that different applications require different levels of support for VPI/VCI usage.**
- **A device that supports 64K VCIs is overkill for the low-cost adapter card market.**
- **Similarly, a device that supports a few VCIs is not suitable for bridge/hub/switch products.**
- **The more VCIs a device supports, the more complex and expensive the device.**

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Driving ATM Into Mainstream Networking

SONET/SDH and ATM The Local Area Network Agenda

- Section 1: Physical layers for ATM*
- Section 2: SONET**/SDH*** as a physical layer for ATM
- Section 3: ATM
- Section 4: ATM and related protocols
- Section 5: TI™ solutions

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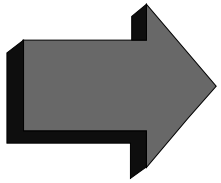
Driving ATM Into Mainstream Networking

ATM and Related Protocols



- **RFC 1577: classical IP and ARP over ATM**
- **LAN emulation**
- **Network management for ATM**

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RFC1577: Classical IP and ARP over ATM

- **Goal: To allow compatible and interoperable implementations for transmitting IP datagrams and ATM ARP requests and replies over AAL5**
- **Describes initial deployment of ATM within classical IP networks as a direct replacement for LANs**
- **“Classical” refers to the treatment of the ATM host adapter as a networking interface to the IP protocol stack**

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RFC1577: Characteristics of the classical model

- **The same maximum transmission unit (MTU) size is used for all VCs in a Logical IP Subnetwork (LIS).**
- **Default logical link control/system network architecture protocol (LLC/SNAP) encapsulation of IP packets**
- **End-to-end IP routing architecture stays the same.**
- **IP addresses are resolved to ATM addresses by use of an ATMARP service within the LIS – ATMARPs (address resolution protocols) stay within the LIS.**
- **One IP subnet is used for many hosts and routers. Each VC directly connects two IP members within the same LIS.**

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RFC 1577

- **Packet format:**
  Support IEEE 802.2 LLC/SNAP encapsulation
- **MTU size:**
  Default MTU size for IP shall be 9180 octets. (RFC-1626 aligns IP over ATM MTU size with that specified for IP over SMDS: RFC-1209) LLC/SNAP = 8 octets; hence, default ATM AAL5 PDU size is 9188 octets.

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RFC 1577 (Continued)

Address resolution:

Uses ATMARP and InATMARP defined in RFC1577; these are based on RFCs 826 and 1293.

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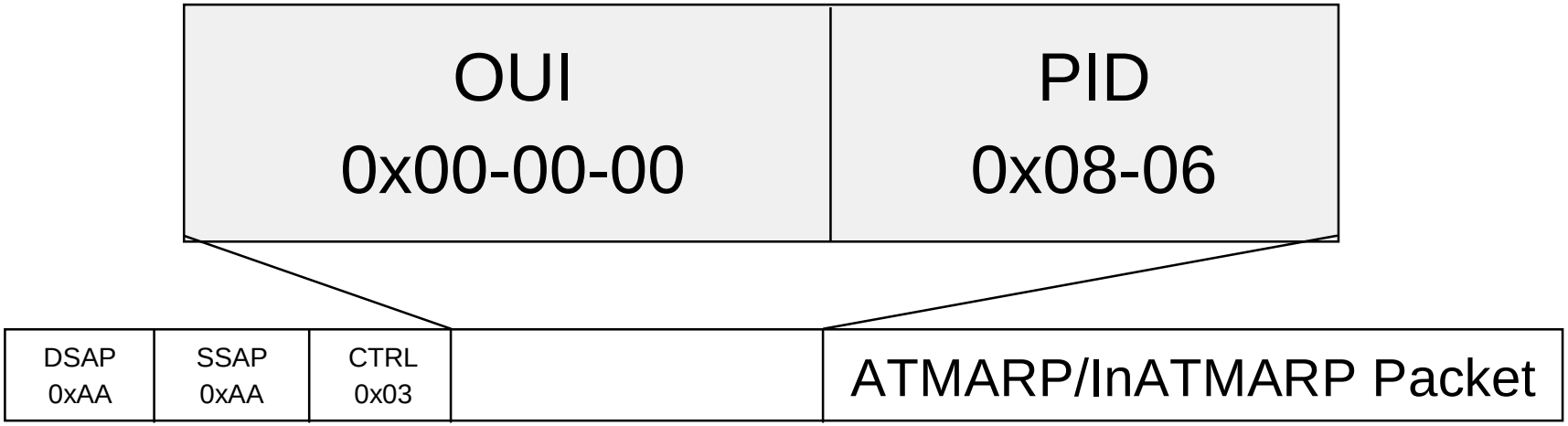
RFC 1577: ATMARP/InATMARP Packet Encapsulation



SNAP Header Values:

OUI = 0x00-00-00 Indicates PID = Ethertype

0x00-00-00-08-06 Ethertype Indicates ARP

The total size of the LLC/SNAP header is fixed at 8 octets. This aligns the start of the ATMARP packet on a 64-bit boundary relative to the start of the AAL5 CPCS-SDU.

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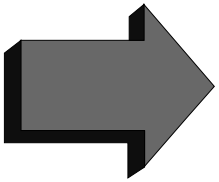
ATM and Related Protocols



- **RFC 1577: classical IP and ARP over ATM**
- **LAN emulation**
- **Network management for ATM**

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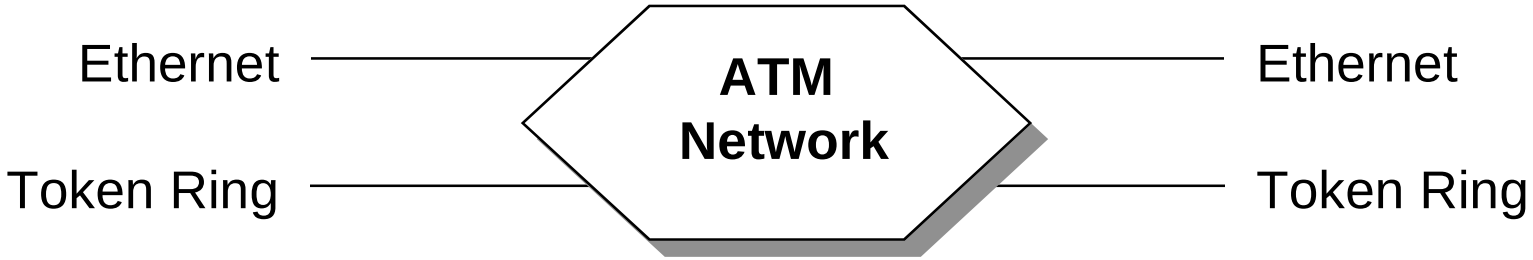
LAN Emulation
The Need and Benefits

- **LAN emulation provides for:**
  - **All existing LAN applications to run over ATM**
  - **The use of ATM as a backbone to interconnect existing legacy LANs**
  - **The interconnection of ATM-attached servers/workstations to each other and to those on legacy LANs**
  - **Multiple-emulated LANs that are logically separate, to use the same physical ATM network**



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LAN Emulation Scope

- **The ATM LAN emulation service should allow equipment such as hosts, desktop computers, bridges, hubs and routers with ATM interfaces to use an ATM network as an extended LAN.**
- **Extended LAN at the MAC layer**
- **Communicate readily with devices on existing LANs, Ethernet, token ring, FDDI, etc.**
- **Functions include:**
  - **Multicast, broadcast, and unicast**
- **Packet delivery exploiting the switching properties and point-to-point nonshared channels of ATM.**

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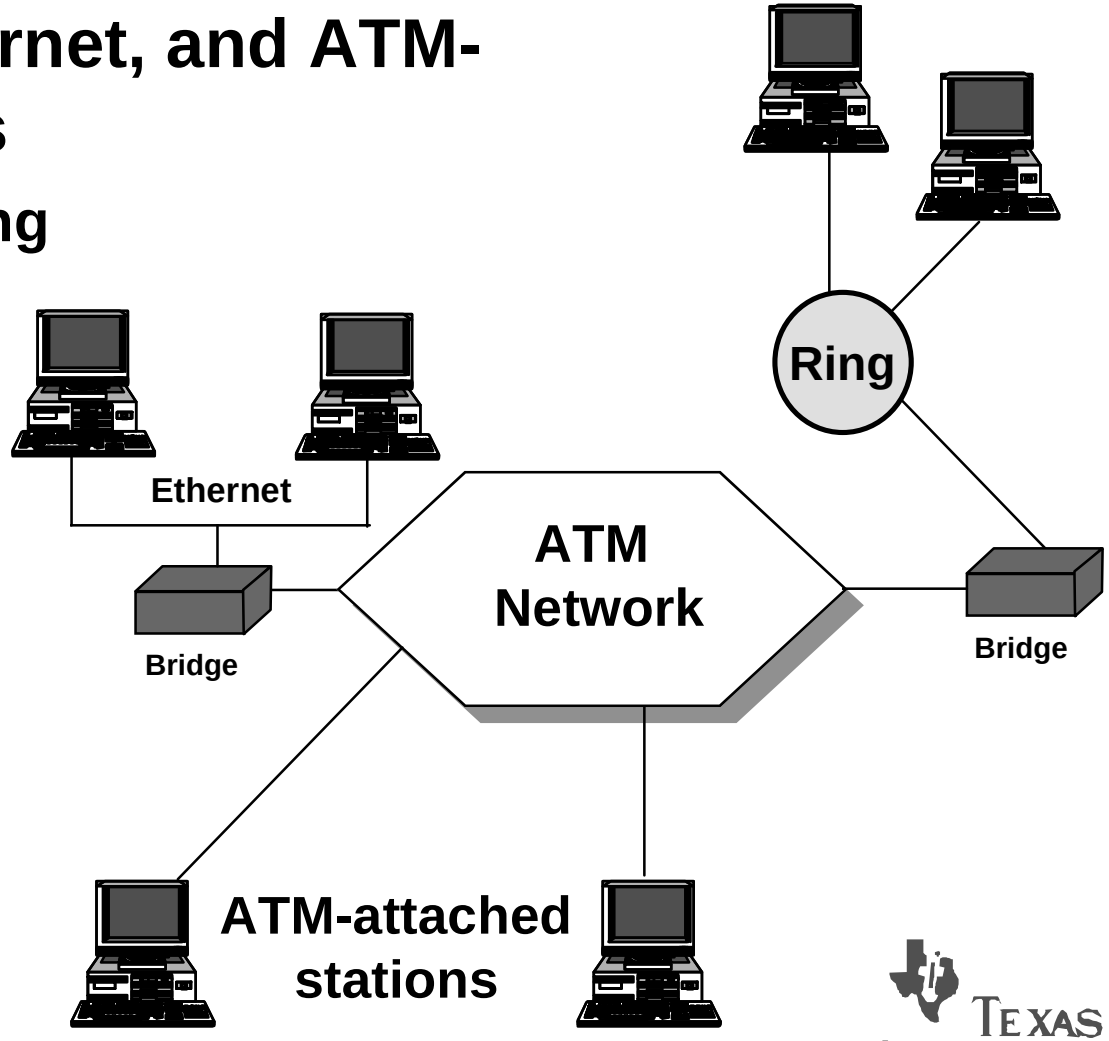
LAN Emulation Scenario

- **An ATM network interconnecting multiple token-ring rings, Ethernet, and ATM-attached end-systems**
  - **Token ring-to-token ring**
  - **Token ring-to-ATM**
  - **Ethernet-to-Ethernet**
  - **Ethernet-to-ATM**
  - **ATM-to-ATM**



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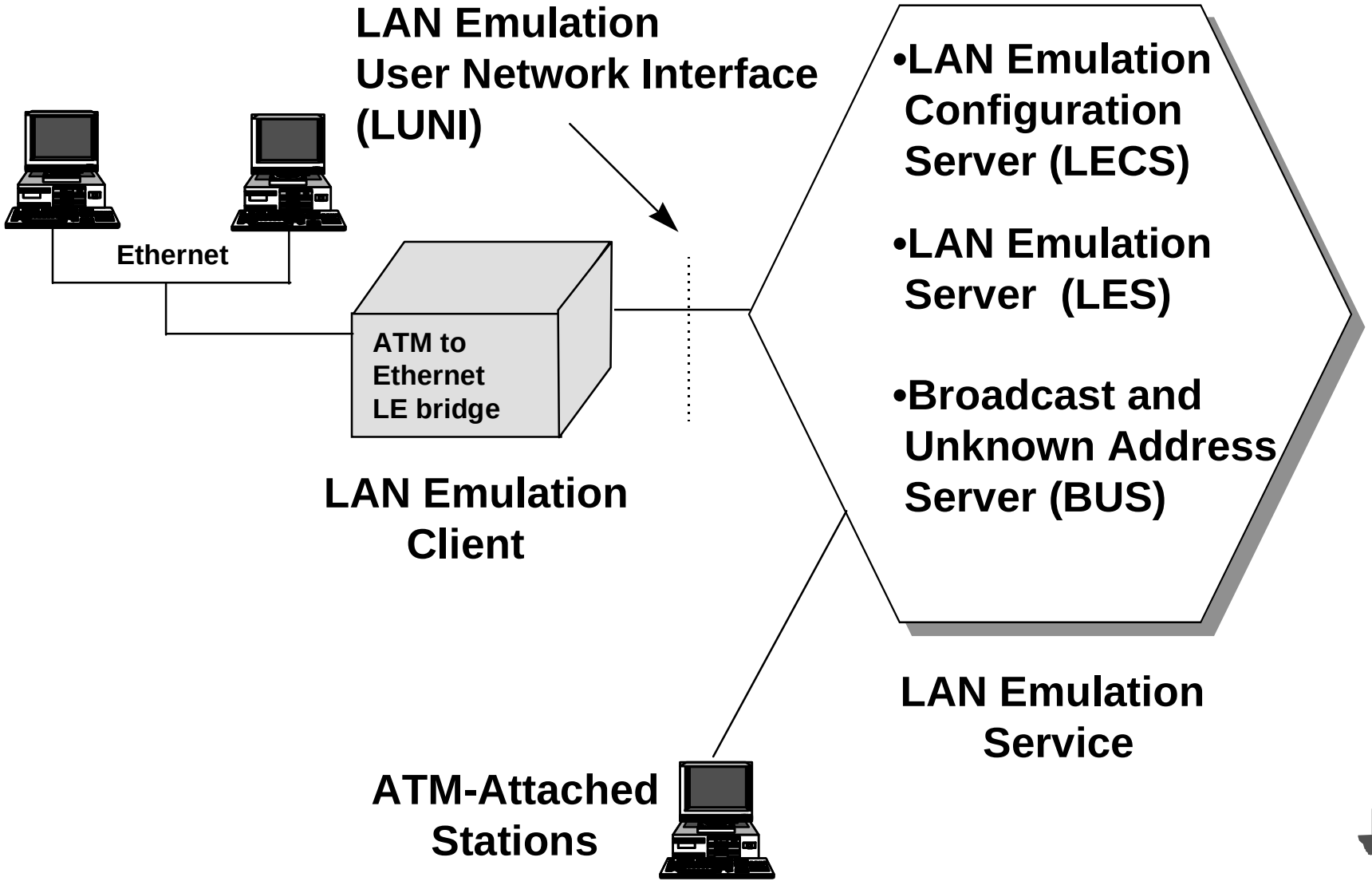
LAN Emulation Scenario



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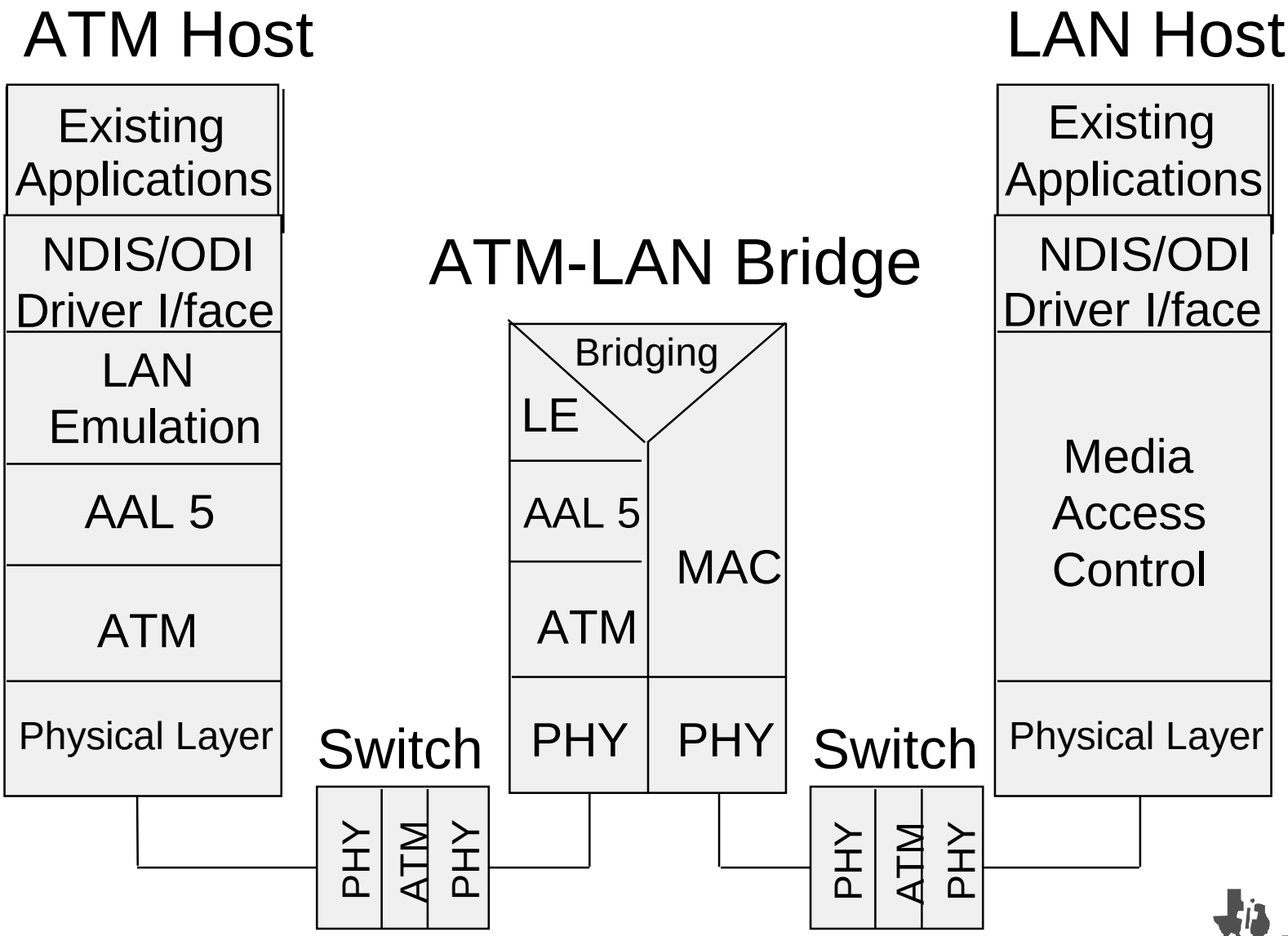
LAN Emulation Protocol Stack



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LAN Emulation Services

- **LE configuration server**
  - **Provides configuration information, address of LE server**
  - **LAN type (token ring or Ethernet)**
  - **MTU (maximum frame size)**
- **LE server**
  - **Implements address registration/resolution functions**
  - **Pairs: MAC address/ATM address**
  - **MAC address and ATM address are unique to an emulated LAN**
- **Broadcast/unknown server**
  - **LE clients use broadcast and unknown server (BUS) for broadcast and multicast**
  - **Handles data sent by LEC-to-MAC broadcast addresses**
  - **Handles data sent by LEC-to-MAC multicast addresses**

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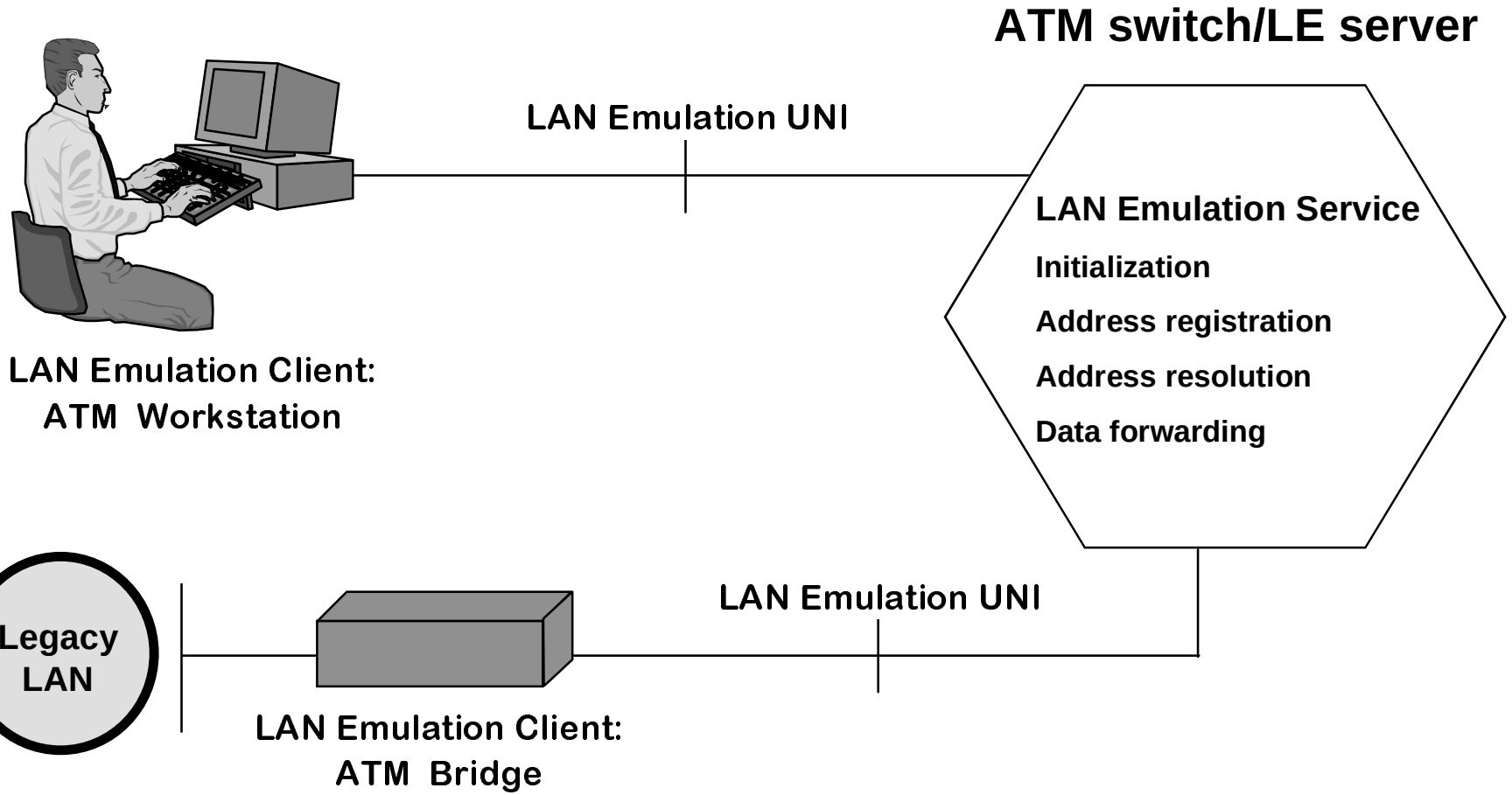
Architecture



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LAN Emulation Control Frames

- **Opcodes control frame types:**
  - **Configuration frames (req. and resp.)**
  - **Join frames (req. and resp.)**
  - **Register & unregister frames (req. and resp.)**
  - **Address resolution frames (req. and resp.)**
  - **Flush frames (req. and resp.)**
  - **Topology change (req.)**
  - **Ready (query and ind.)**
- **Each opcode (frame type) has an associated protocol and packet format defined.**

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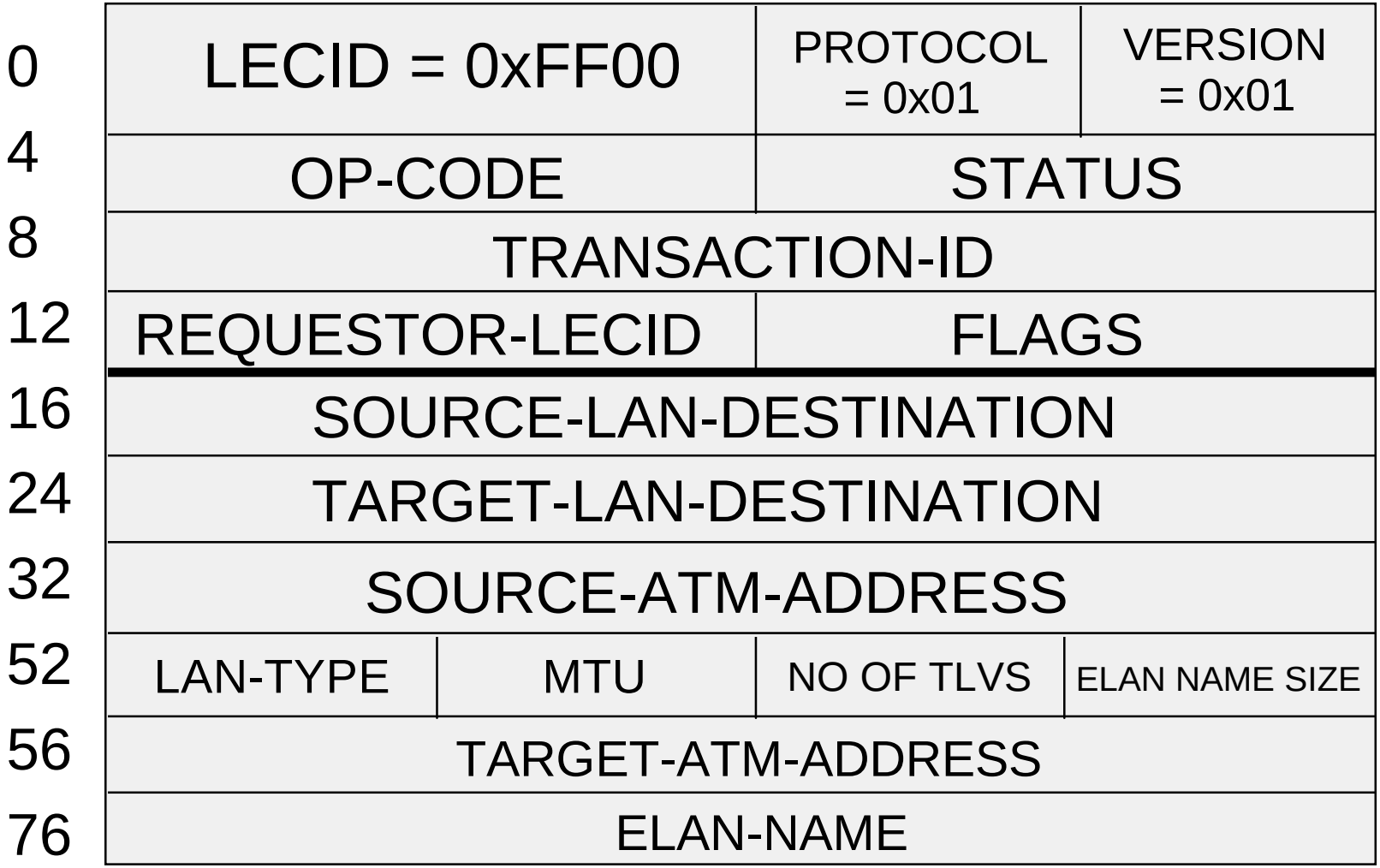
LAN Emulation Control Frames



108 (byte offsets)

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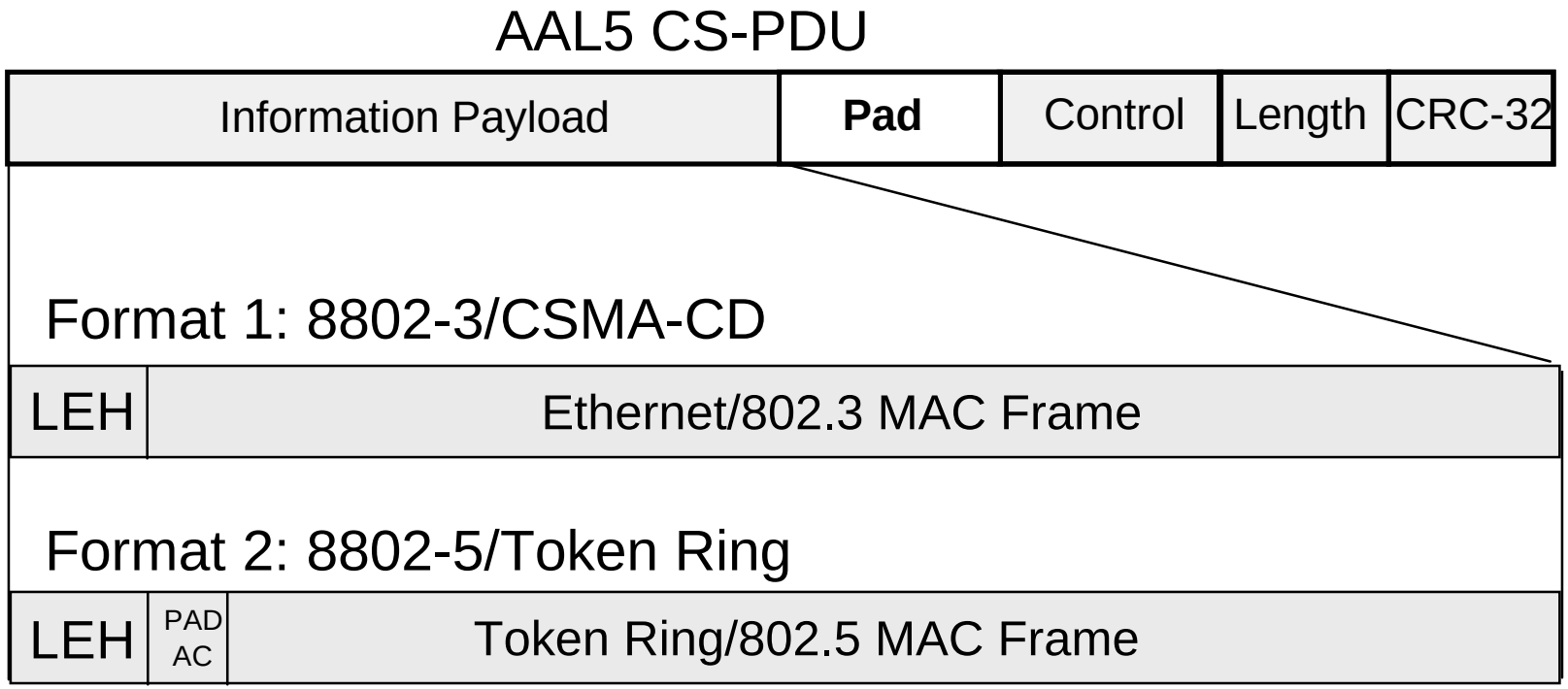
LAN Emulation: Data Frames



Byte after LEH can be any PAD value; e.g., 802.5 AC field, MAC frame starts with FC byte

LEH: Fixed Length, LAN emulation header, two bytes

FDDI bridging rules to either are well-defined

Note: No MAC FCS

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Emulated LAN Types

- **Emulated LAN provides the functionality of a single LAN segment:**
  - **Ethernet/802.3 segment**
  - **Token ring/802.5 segment**
- **Emulated LAN does not emulate all segment specific details of the emulated LAN type:**
  - **No collisions**
  - **No tokens, no beacon frames**
  - **Legacy maximum frames sizes do not apply.**

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LAN Emulation Summary

- **Single ATM adapter card in a server could provide for n emulated Ethernet segments.**
- **The goal is to have no impacts on LAN operating system drivers; i.e., existing Ethernet NOS modules would be used for emulated Ethernets.**
- **Hence LAN emulation drivers would interface to existing protocol stacks with no changes.**
- **Broadband-ISDN application program interfaces would complement LAN emulation drivers to provide access to native ATM functions.**

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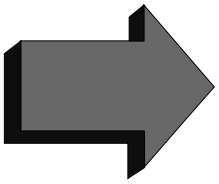
ATM and Related Protocols

- **RFC 1483: multiprotocol encapsulation over ATM adaptation layer 5**
- **RFC 1577: classical IP and ARP over ATM**
- **LAN emulation**
- **Network management for ATM**



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Driving ATM Into Mainstream Networking

SONET/SDH and ATM The Local Area Network Agenda

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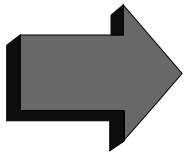
TI Solutions



- **ATM SAR Solutions**
- **ATM PHY Solutions**
- **Applications**
- **Evaluation Kits**
- **Contacts**

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ATM SAR Devices: TNETA1570

TNETA1570 - HyperSAR

- Designed for 200 Mbit/s throughput systems
- Early segmentation feature (buffer segmentation, not packet)
- Integrated 64-/32-bit PCI host interface (PCI spec. Rev 2.0, ’93)
- Supports full range of VPIs (12 bits) for NNI
- Can support 30720 VCIs for a single VPI
- Simultaneous seg./reassem. of up to 1023/30720 packets
- 240-pin MQUAD package
- Samples now
- Evaluation board now

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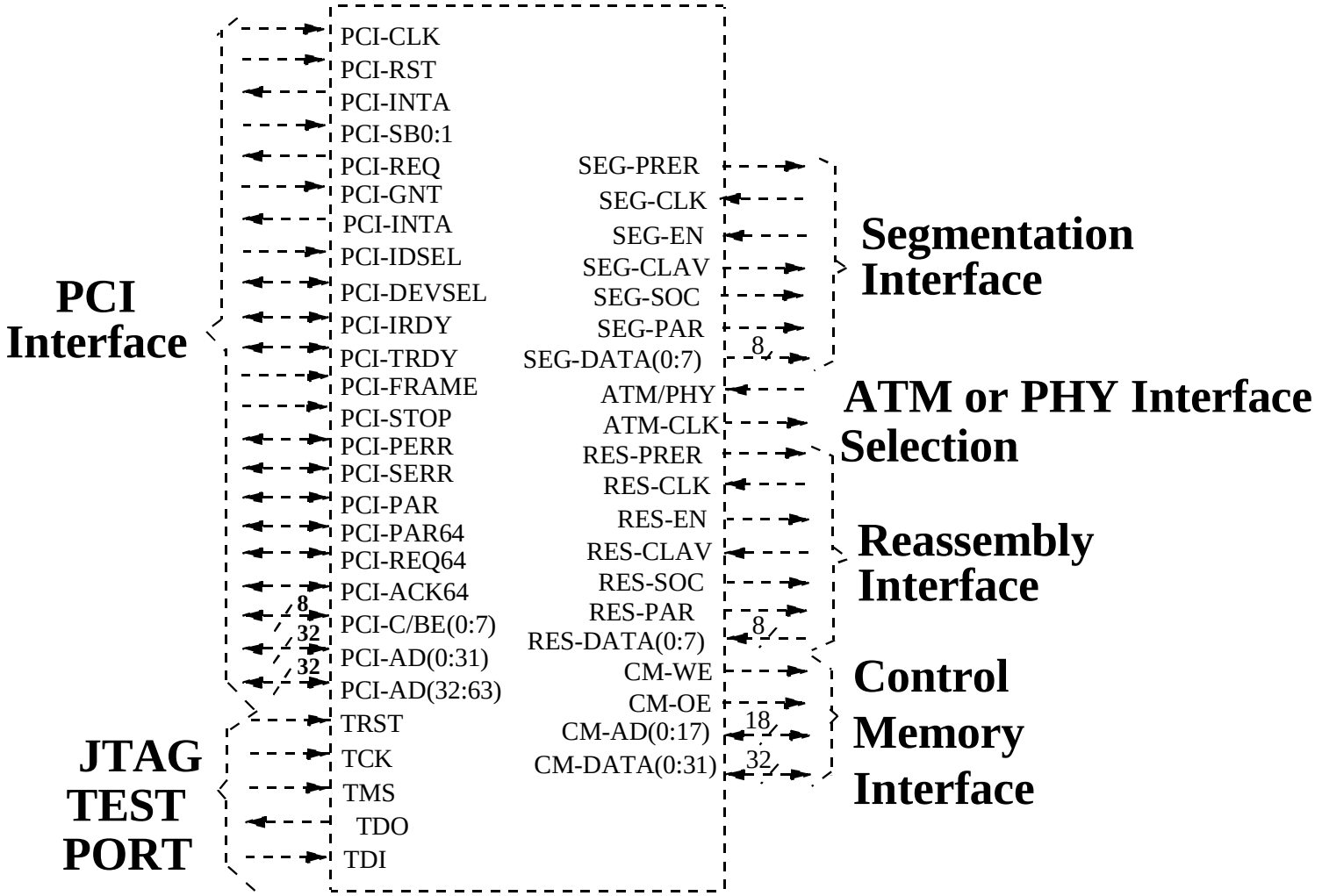
TNETA1570 HyperSAR Interfaces



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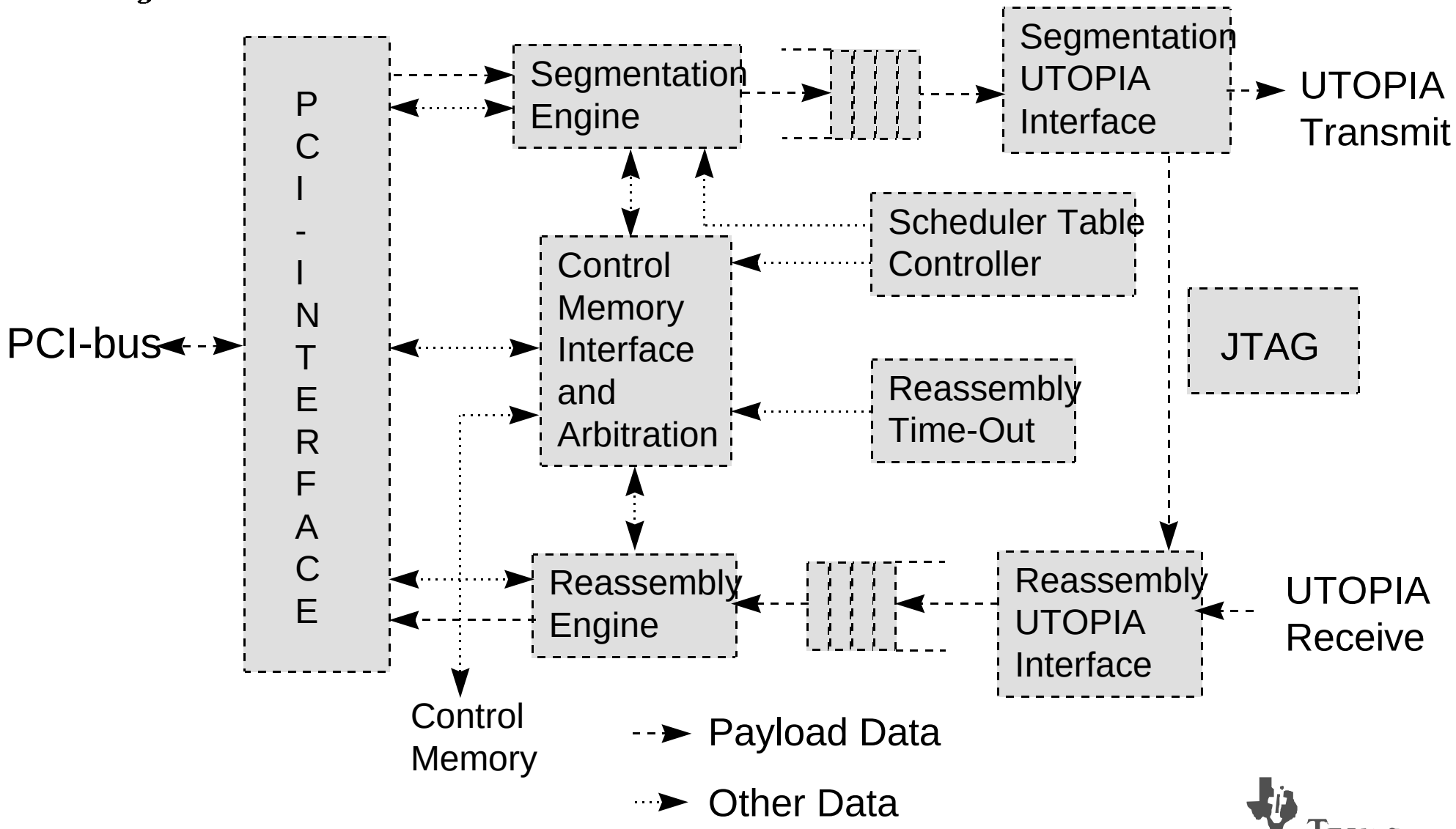
HyperSAR Architecture
Driving ATM into Mainstream Networks



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ATM SAR Devices: TNETA1561

TNETA1561 - PCI Bus SAR

- Integrated 32-bit PCI host interface (PCI spec. Rev 2.0, 1993)
- PCI configuration space built into the device
- Aimed at 155 Mbit/s file server for legacy clients and workstation ATM client market
- Integrated FIFOs sized for low-cost workstation applications
- High-performance DMA bus mastering (48-byte bursts)
- Efficient gather function for LAN emulation implementation
- Big endian/little endian option for embedded applications
- 240-pin MQUAD package
- Samples now
- Evaluation board now

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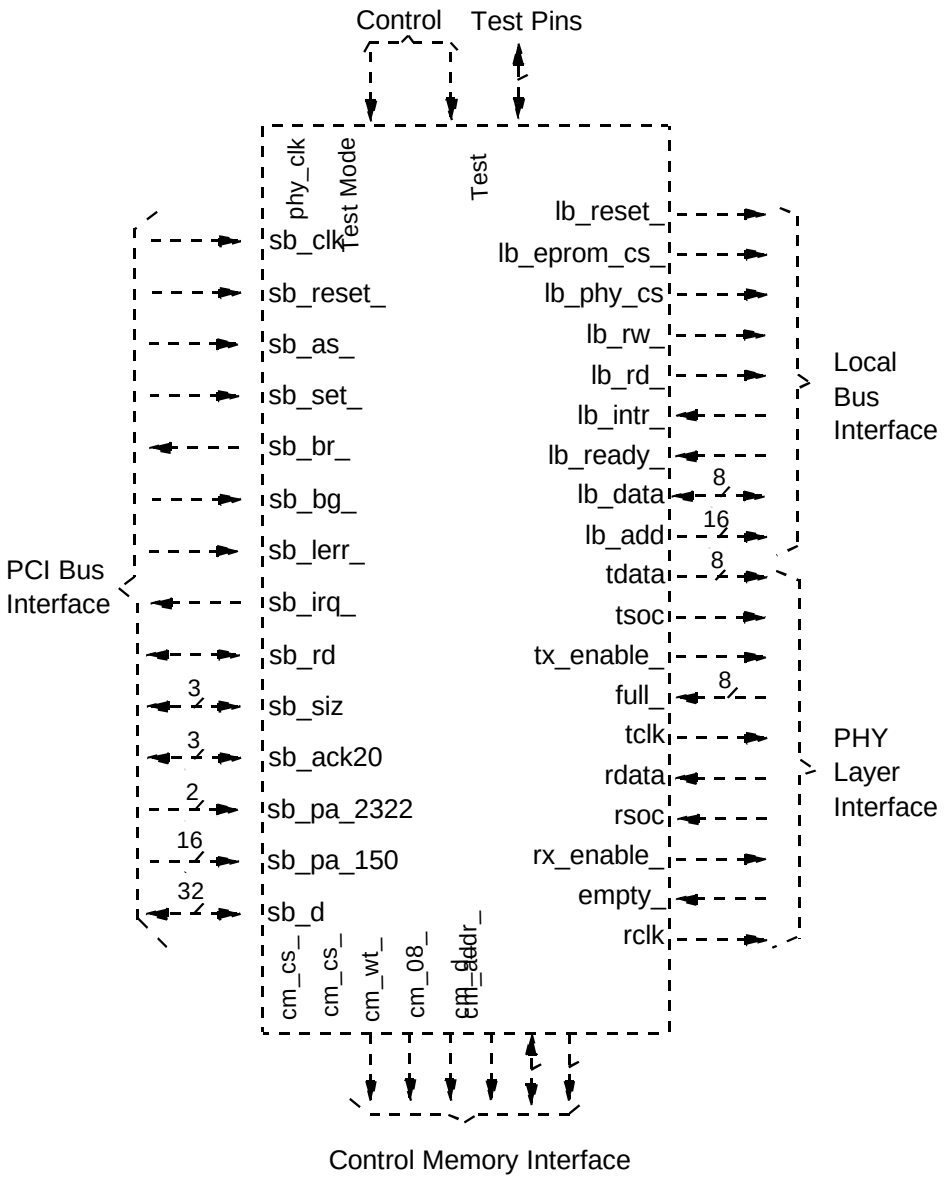
TNETA1561 PCI Bus SAR Interfaces



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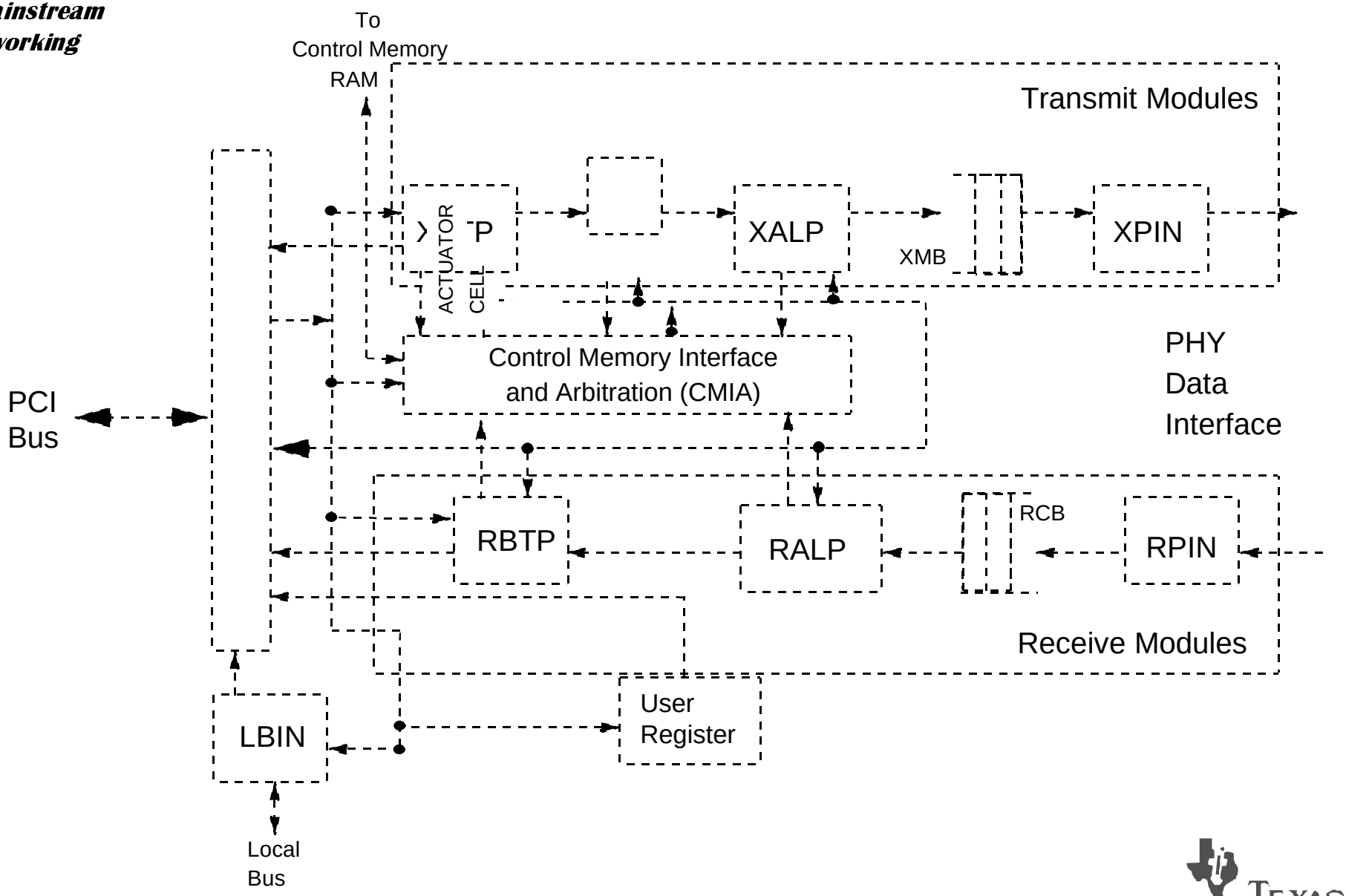
PCI Bus SAR Architecture



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ATM SAR Devices: TNETA1560

TNETA1560 - SBus SAR

- Integrated 32-bit SBus host bus interface (IEEE1496-1993)
- Aimed at 155 Mbit/s file server for legacy clients and work station ATM client market
- Integrated FIFOs sized for low-cost workstation applications
- Cell payloads are stored in host memory, not local SRAM
- High-performance DMA bus mastering (32- and 16-byte bursts)
- Efficient gather function for LAN emulation implementation
- Compliant to the UTOPIA specification
- 240-pin MQUAD package
- Samples available now
- Evaluation board available now

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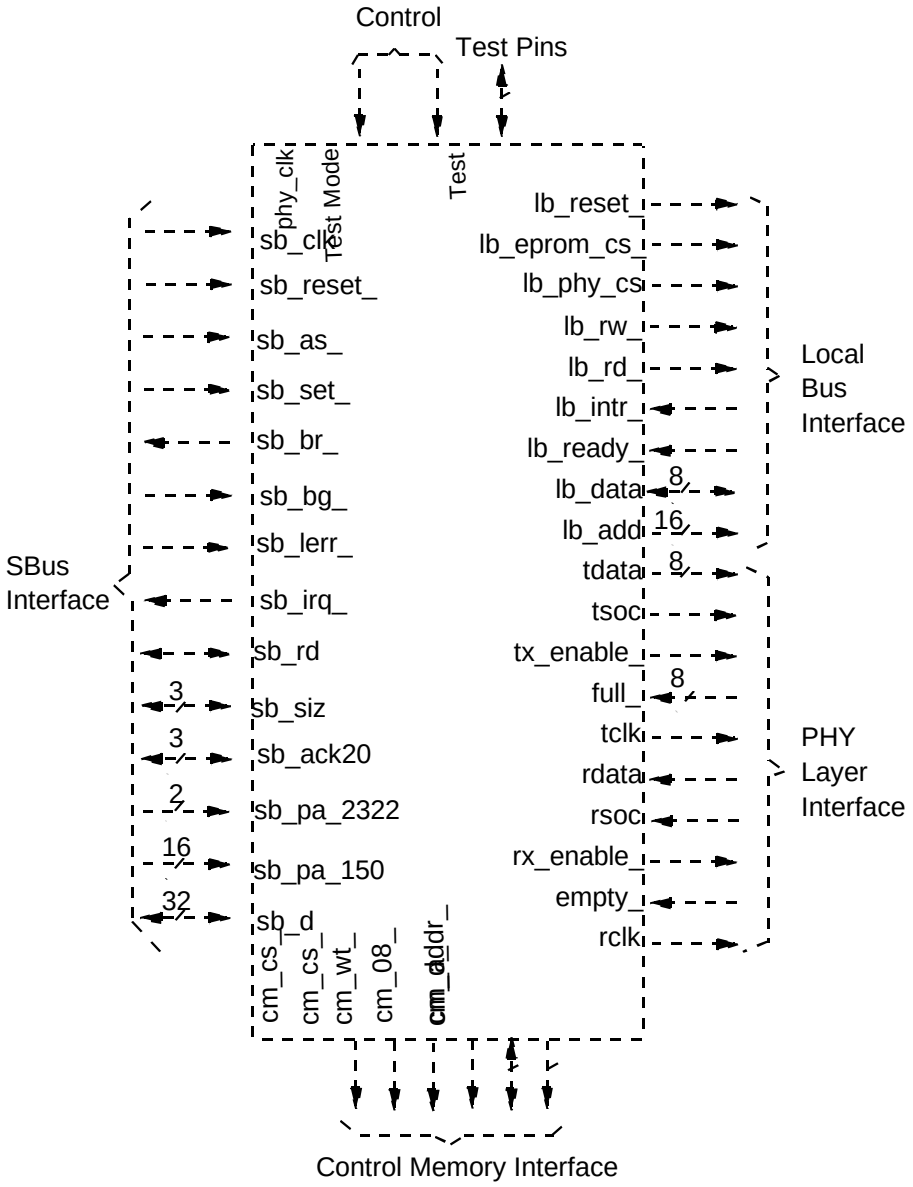
TNETA1560 SBus SAR Interfaces



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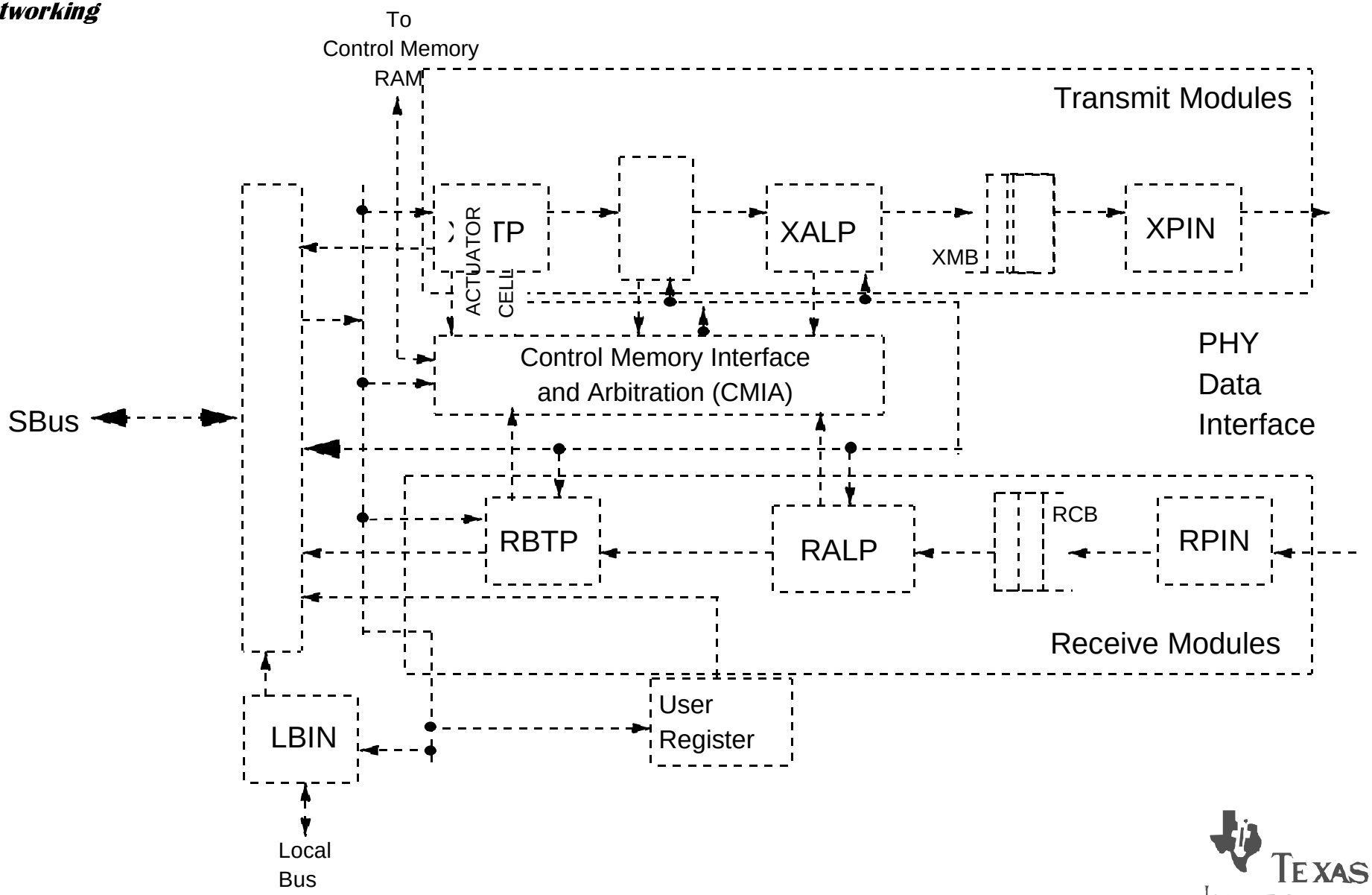
SBus SAR Architecture



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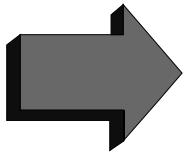
TI Solutions



- ATM SAR solutions
- ATM PHY solutions
- Applications
- Evaluation kits
- Contacts

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Driving ATM Into Mainstream Networking

ATM PHY Devices: TNETA1500

TNETA1500 – 155 Mbit/s Single-Chip ATM PHY

- Provides clock generation/clock recovery
- External 19.44 MHz clock source
- Inserts/extracts ATM cells into/from SONET and SDH frames
- Detects multiple-bit errors and corrects single-bit errors
- Generates alarms for various error conditions, LOS, etc.
- Meets ATM Forum UNI specification
- Compliant to the UTOPIA specification
- Samples available now in 144-pin PQFP
- Evaluation board available now

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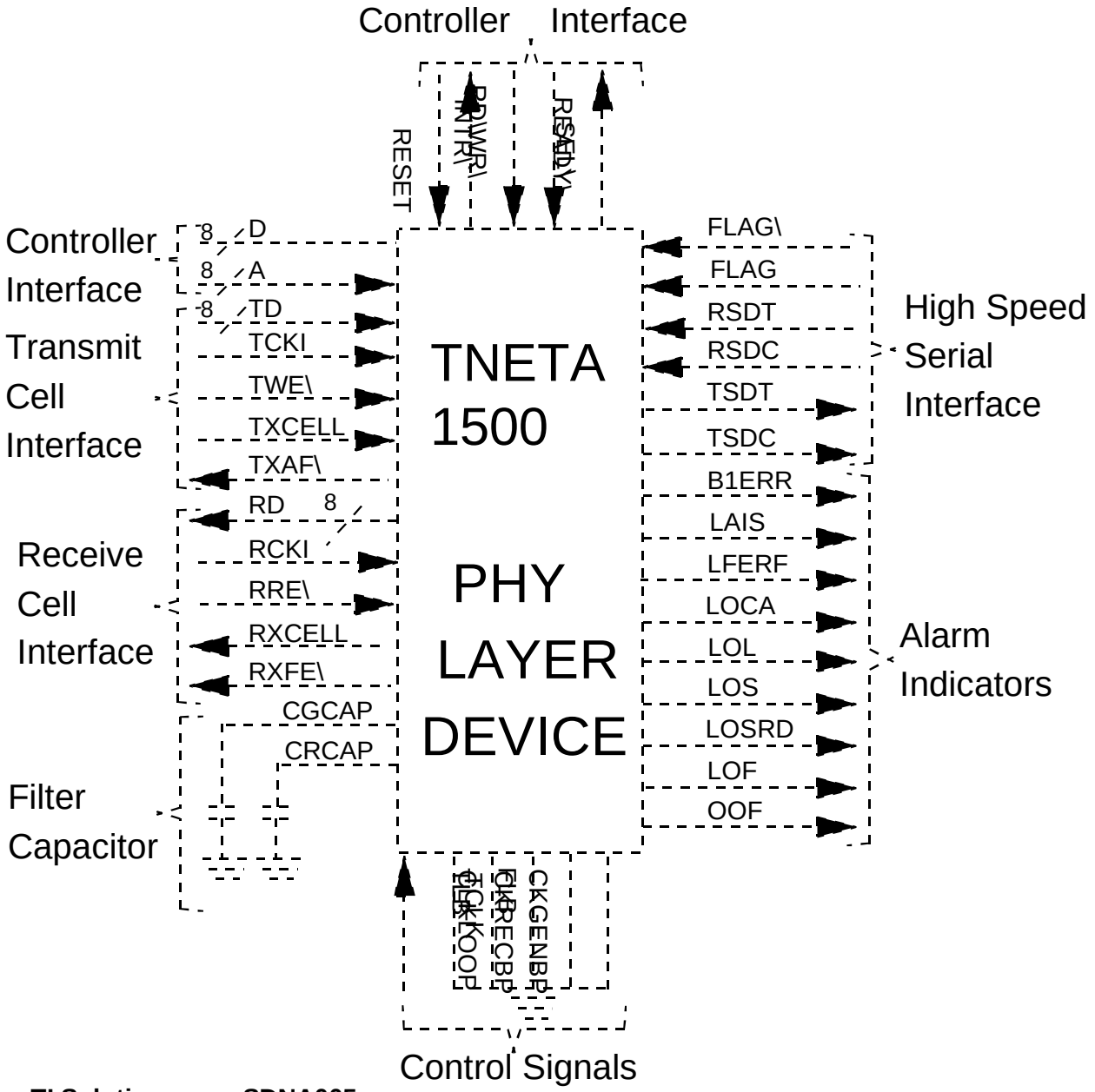
Driving ATM Into Mainstream Networking

TNETA1500 SABRE™



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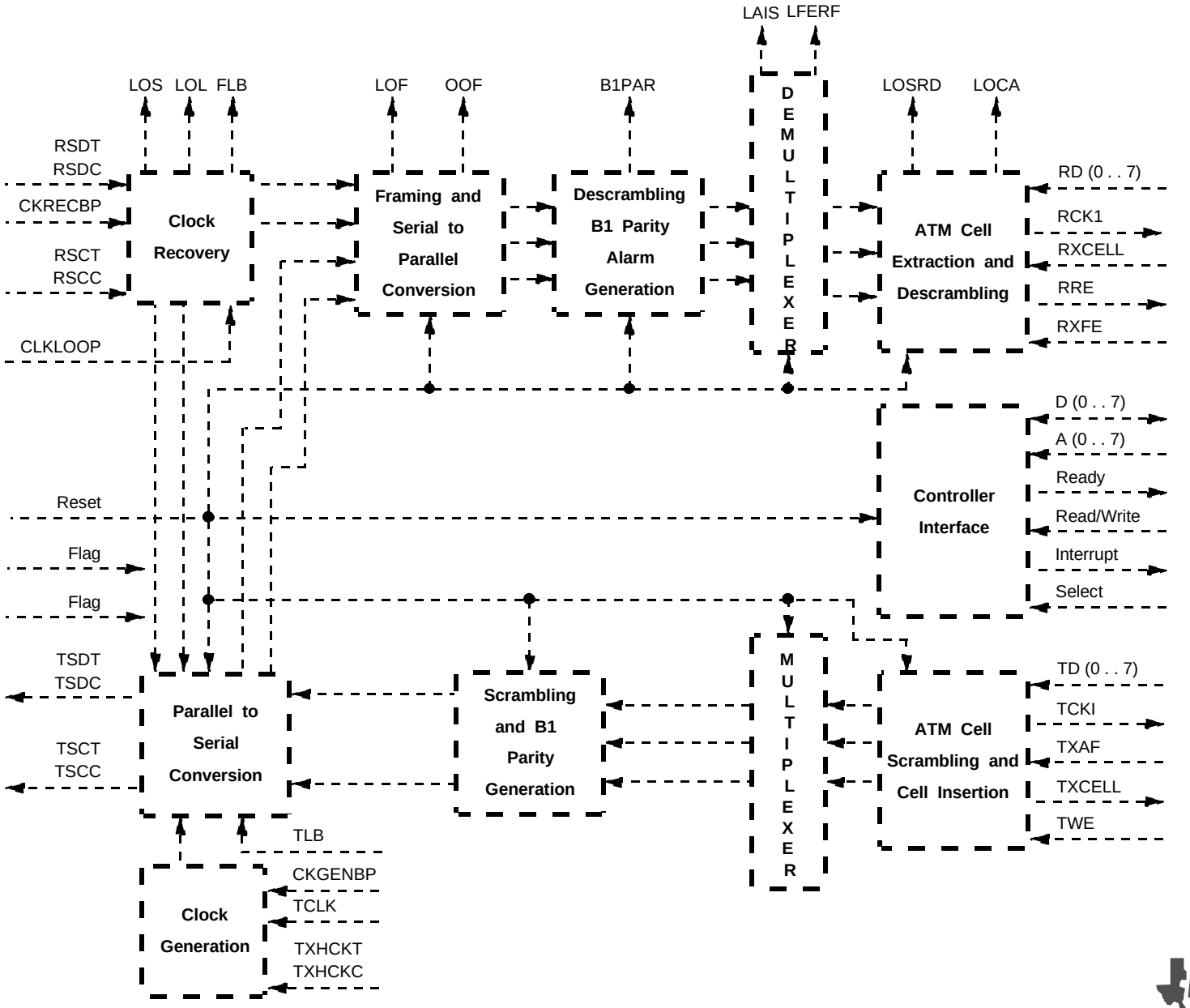
TNETA1500 Architecture



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ATM PHY Devices: TNETA1600

TNETA1600 – 155/622 Mbit/s SONET/SDH Overhead

- Termination/generation and Mbit/s processor
- Operates at 622 or 155 Mbit/s
- Generation/termination of SONET STS-3c & STS-12c and SDH STM-1 and STM-4c frames carrying ATM cells
- 8-/16-bit UTOPIA interface
- Access to all SONET/SDH overhead bytes for both Tx and Rx
- Access to datacom and orderwire overhead bytes
- JTAG functionality – IEEE Std 1149.1-1990

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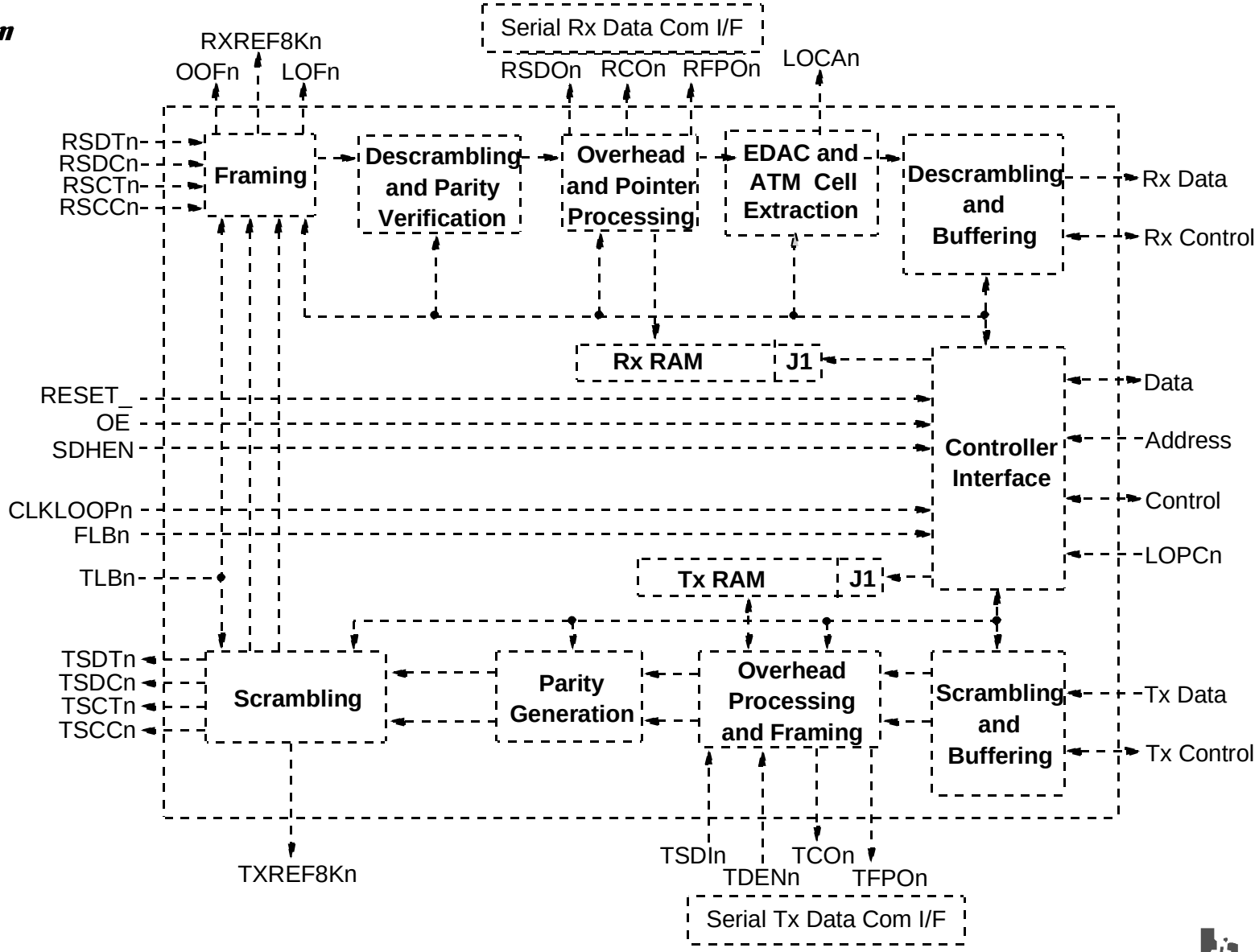
TNETA1600 Architecture



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ATM PHY Devices: TNETA1610

TNETA1610 – 622-Mbit/s Line Interface

- Built-in clock recovery/clock generation
- 19.44-MHz clock source
- Serial/parallel – parallel/serial conversion
- Align byte-wide output data with A1 byte boundaries
- Full framing function completed by TNETA1600
- Alarm codes – LOPC (loss-of-optical carrier)

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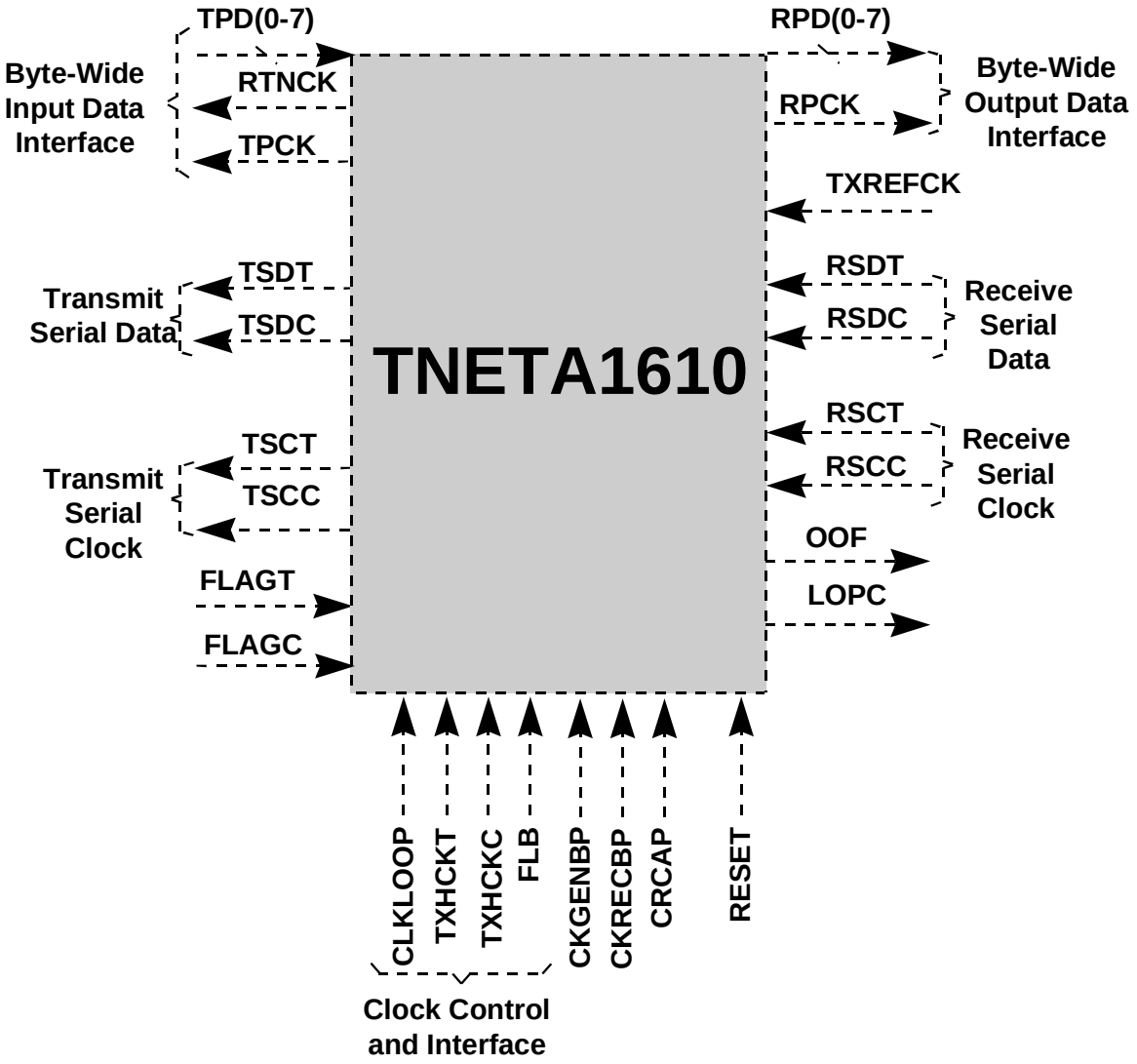
TNETA1610 Interfaces



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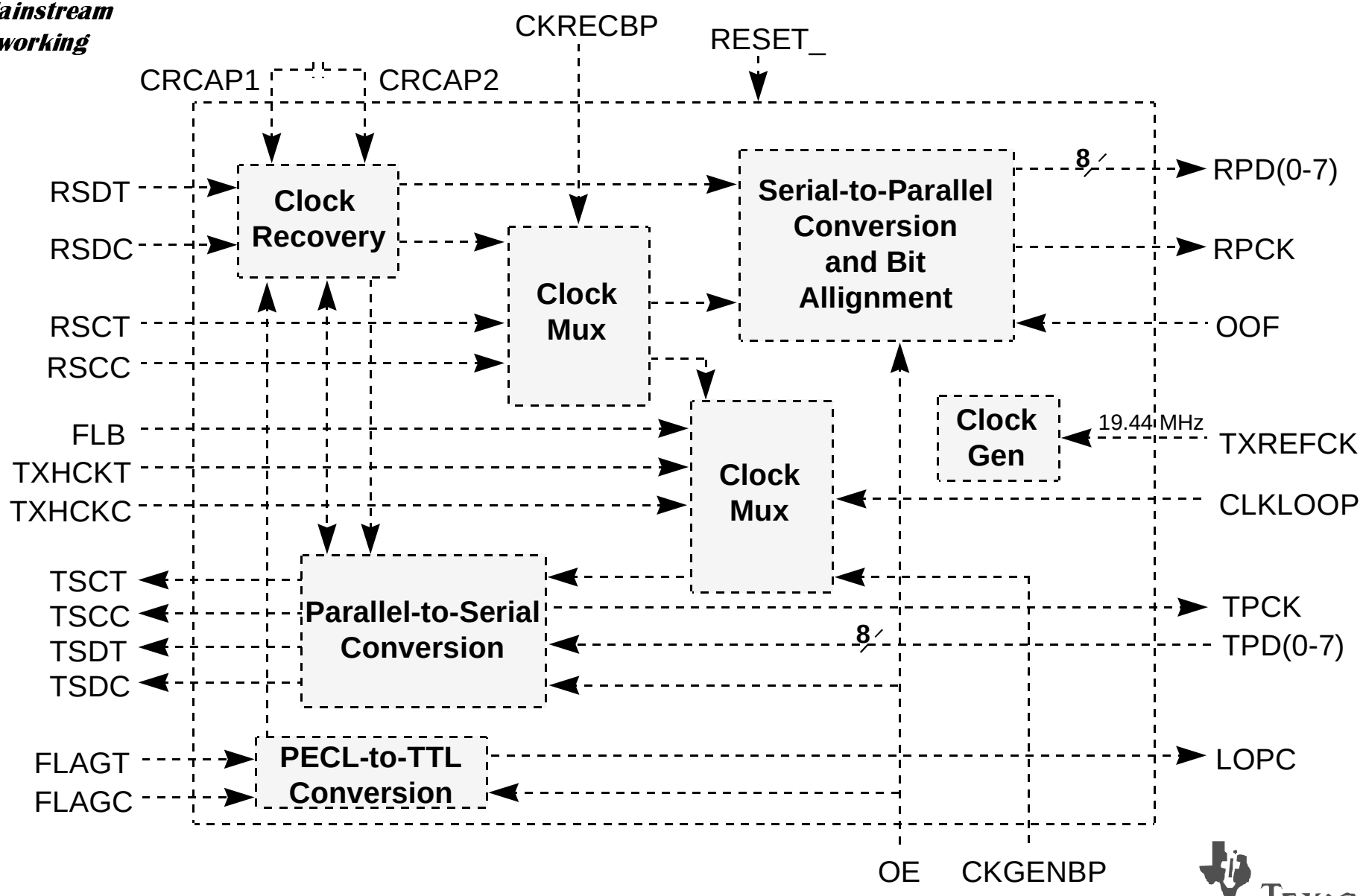
TNETA1610 Architecture



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ATM PHY Devices: TNETA1611

TNETA1611 – 622-Mbit/s Line Interface

- 19.44-MHz clock source
- Serial/parallel – parallel/serial conversion
- Align byte-wide output data with A1 byte boundaries
- Full framing function completed by TNETA1600
- Alarm codes – LOPC (loss-of-optical carrier)
- Samples available now

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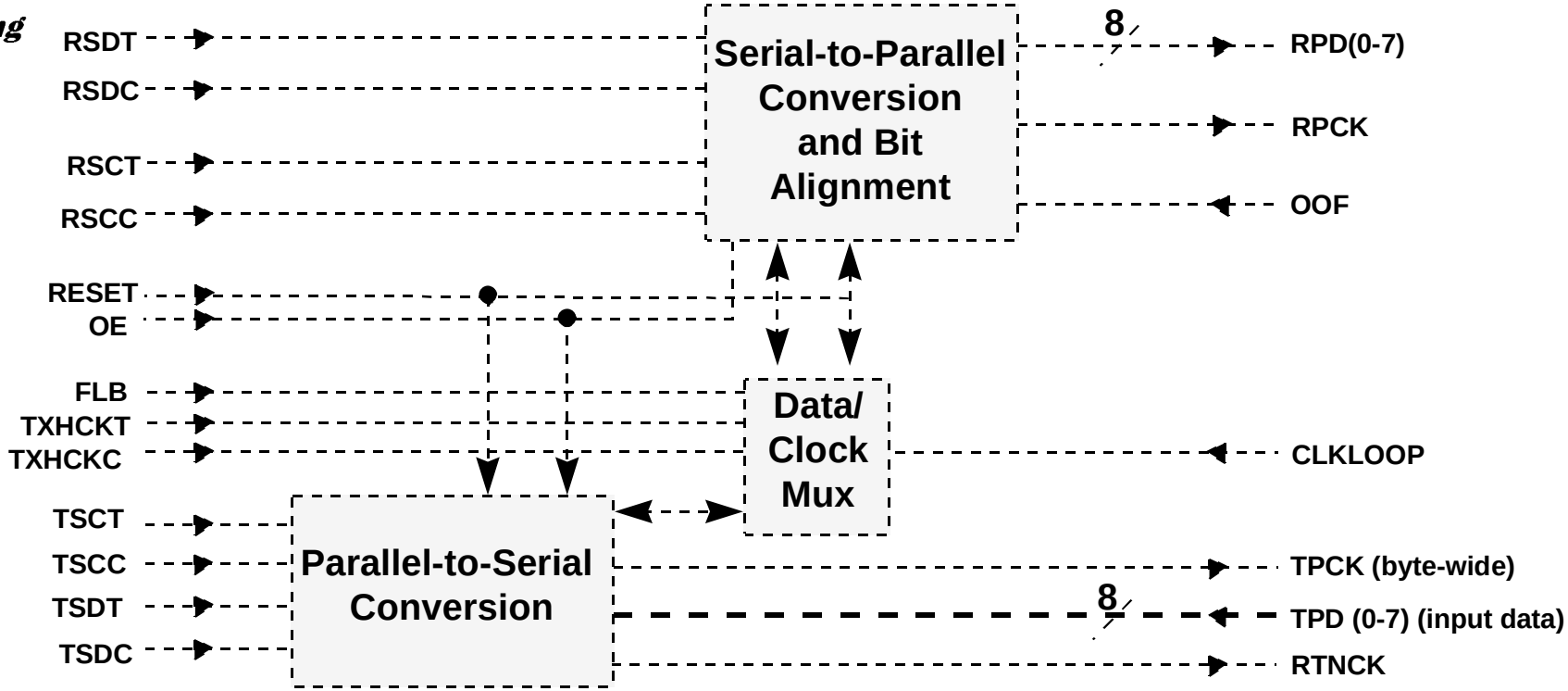
Driving ATM Into Mainstream Networking

TNETA1611 Architecture



- Serial-to-Parallel/Parallel-to-Serial Conversion for 622.08-Mbit Data Streams
- Transmit Clock Source is Selected From External Clock Source or Receive Clock Input
- Performs Bit-Alignment Function for SONET/SDH Frames
- Loopback Capability increases Product Versatility
- Conforms to SONET/SDH Standards

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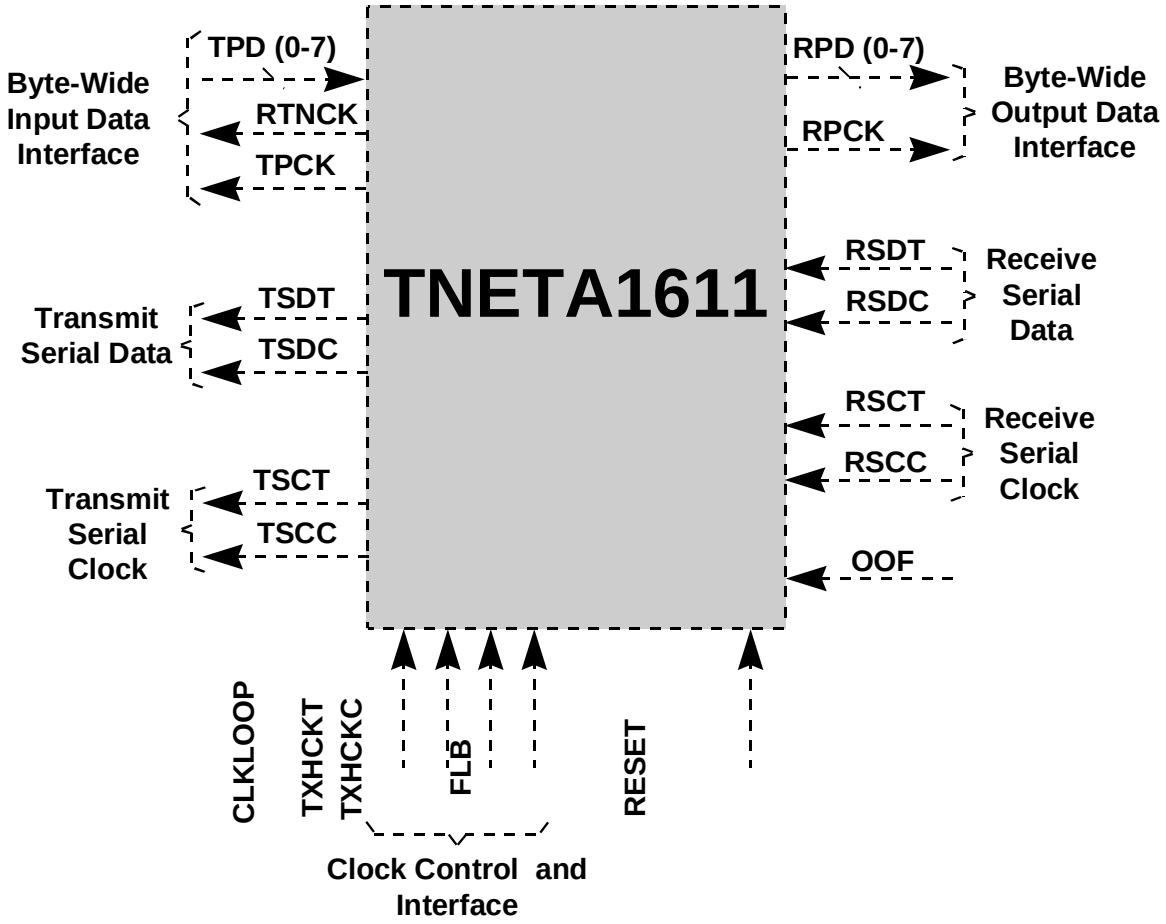
Driving ATM Into Mainstream Networking

TNETA1611 Interfaces



The TNETA1611 is an STS-12c/STM-4 receiver/transmitter that performs data serialization and deserialization for 622.08-Mbit/s data streams used in STS-12c/STM-4 systems. On the receive side, bit alignment is performed on the serial input so parallel data is output on SONET/SDH byte boundaries. The TNETA1611 conforms to applicable SONET/SDH standards and simultaneously converts the serial data to and from byte-wide data. Clock and data loopback are included to increase versatility.

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Driving ATM Into Mainstream Networking

ATM PHY Devices: TNETA1622

TNETA1622 – 622-Mbit/s clock recovery

- Recovers a 622.08-MHz clock signal from a 622.08-Mbit/s STS-12c/STM-4c NRZ data stream
- Accepts PECL input voltage levels on input data stream
- Requires single 5-V supply
- Provides PECL clock and data outputs
- Meets stringent Bellcore jitter specifications
- 20-pin plastic small-outline DW package
- Samples available July 1995
- Evaluation Board July 1995

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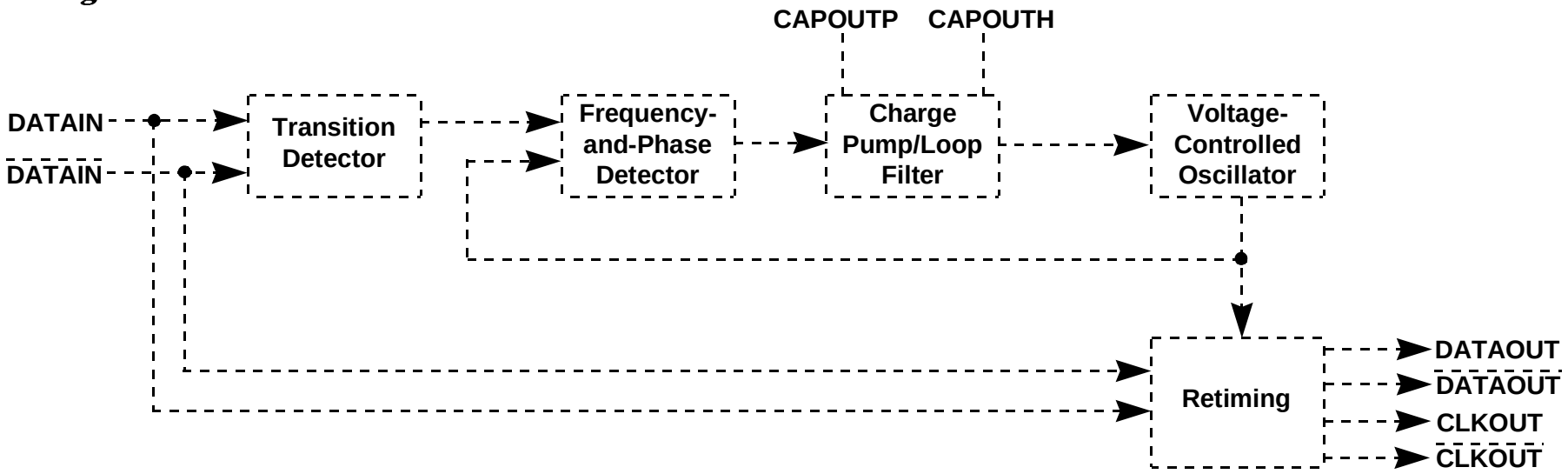
Driving ATM Into Mainstream Networking

TNETA1622 Architecture



The TNETA1622 recovers an embedded clock signal from a 622.08-Mbit/s STS-12/STM-4 nonreturn-to-zero (NRZ) data stream using a frequency/phased-locked loop. The device accepts PECL (ECL signals referenced to 5 V instead of GND) input-voltage levels. The recovered clock and data outputs are PECL compatible. The serial data input and recovered clock and data outputs are differential to provide maximum noise immunity.

The TNETA1622 requires only a positive 5-V supply operation over a temperature range of

-40^{o}C to 85^{o}C.

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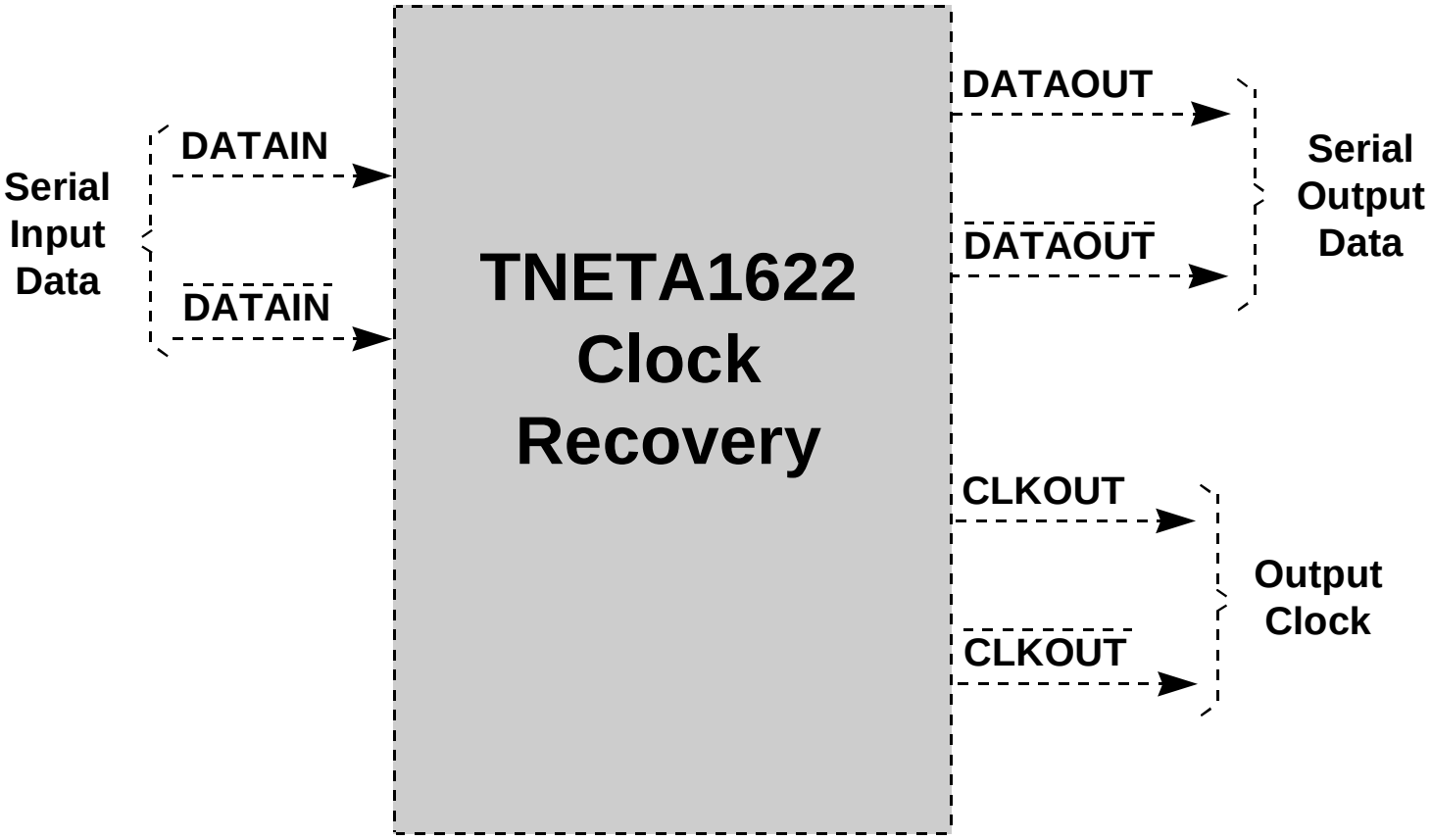
TNETA1622 Interfaces



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Driving ATM Into Mainstream Networking

ATM PHY Devices: TNETA1630

TNETA1630 – 622-Mbit/s Clock Generation.

- Generates a 622.08-MHz clock from a TTL clock of 19.44Hz
- Provides differential psuedo-ECL (PECL) outputs
- Requires single 5-V supply
- Meets stringent Bellcore jitter specifications
- 20-pin plastic small-outline DW package
- Production released
- Evaluation board available now

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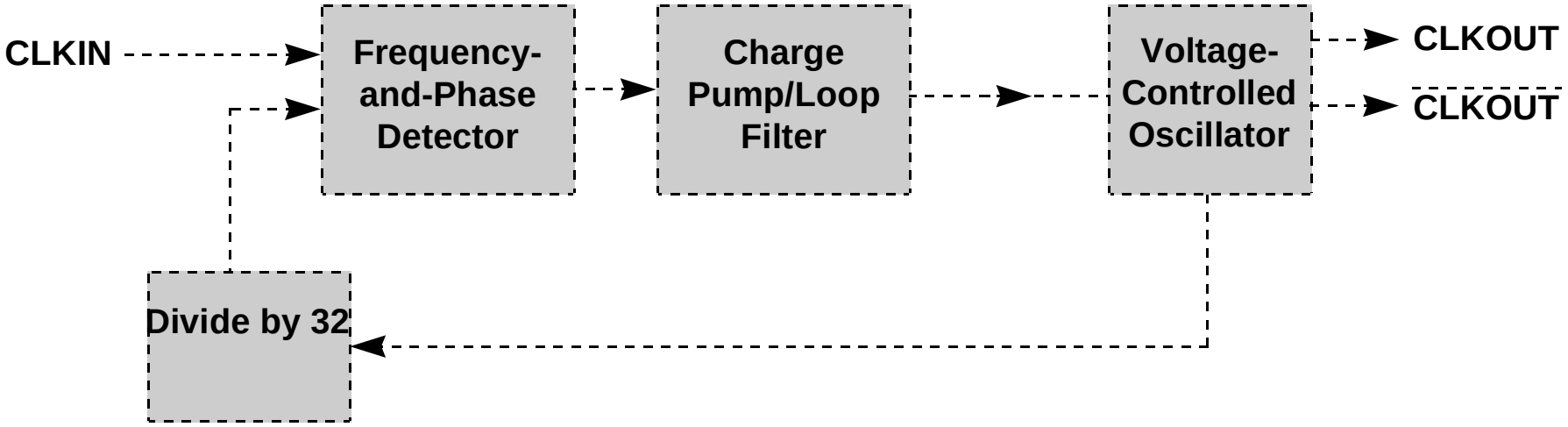
Driving ATM Into Mainstream Networking

TNETA1630 Architecture



The TNETA1630 is a 622.08-MHz clock-generation device that utilizes a TTL-clock input at 19.44 MHz. The 622.08-MHz clock is provided on differential pseudo-ECL (PECL) outputs. The TNETA1630 operates from a single 5-V power supply. An internal second-order low-pass filter is used to reduce jitter.

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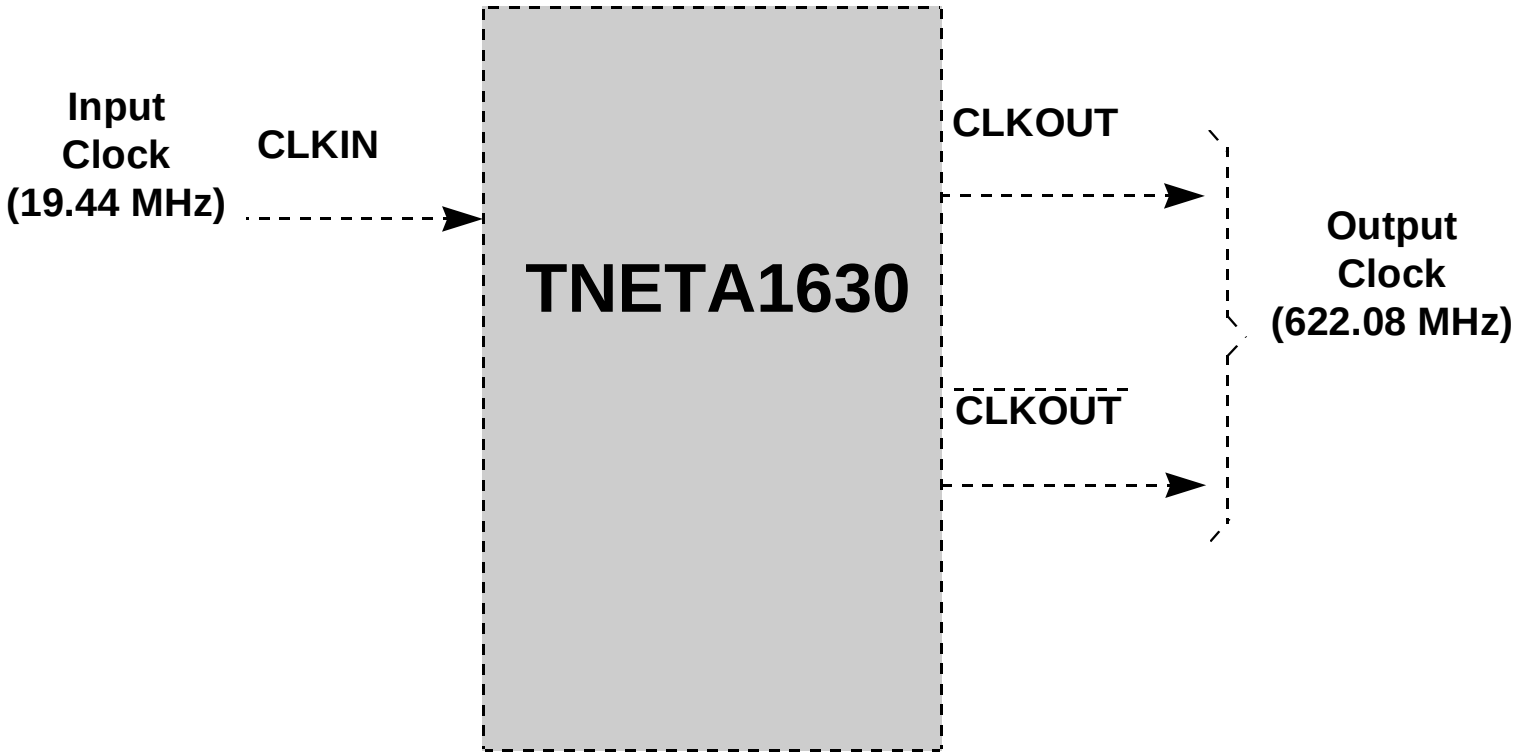
TNETA1630 Interfaces



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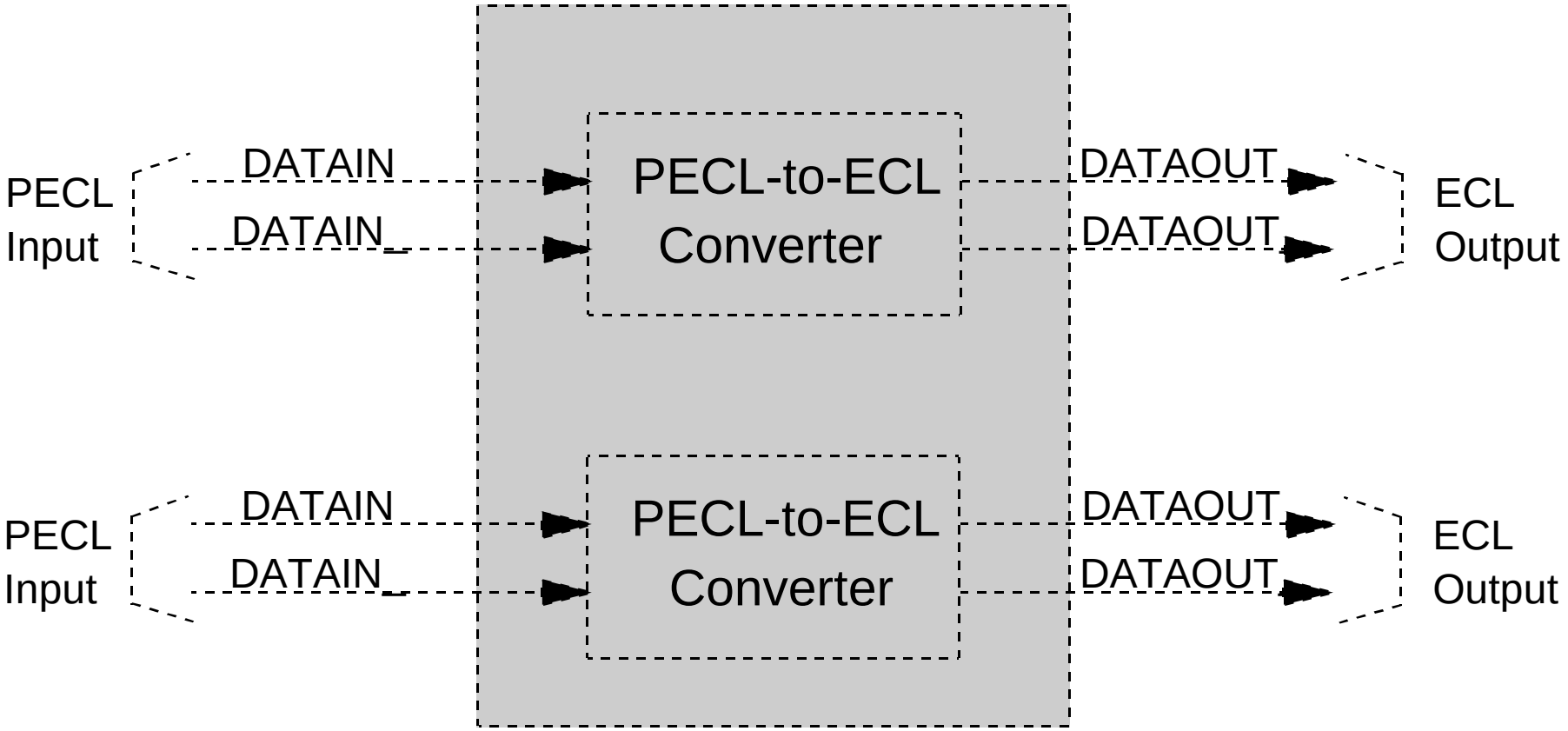
TNETA1545
PECL : ECL Level Shifter



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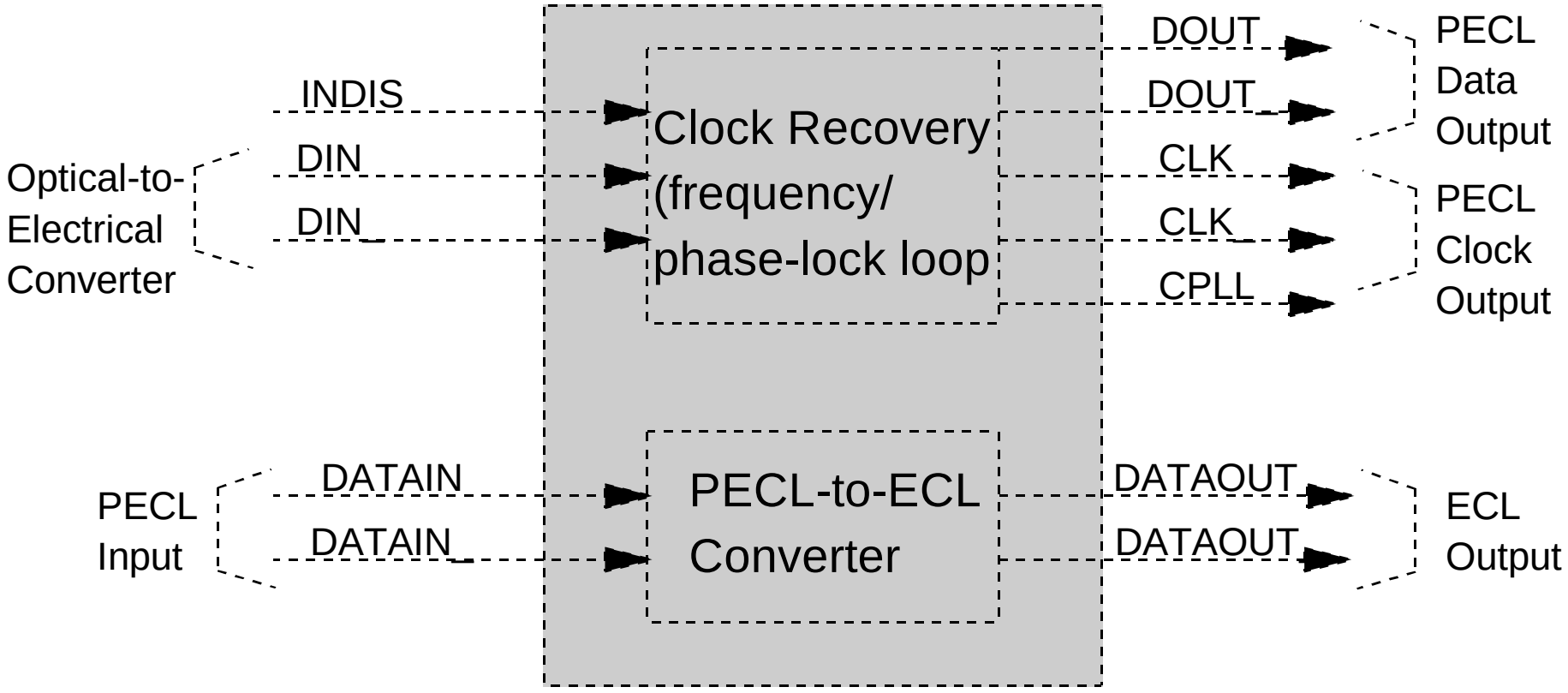
TNETA1555 – 155.52-MHz Clock Recovery



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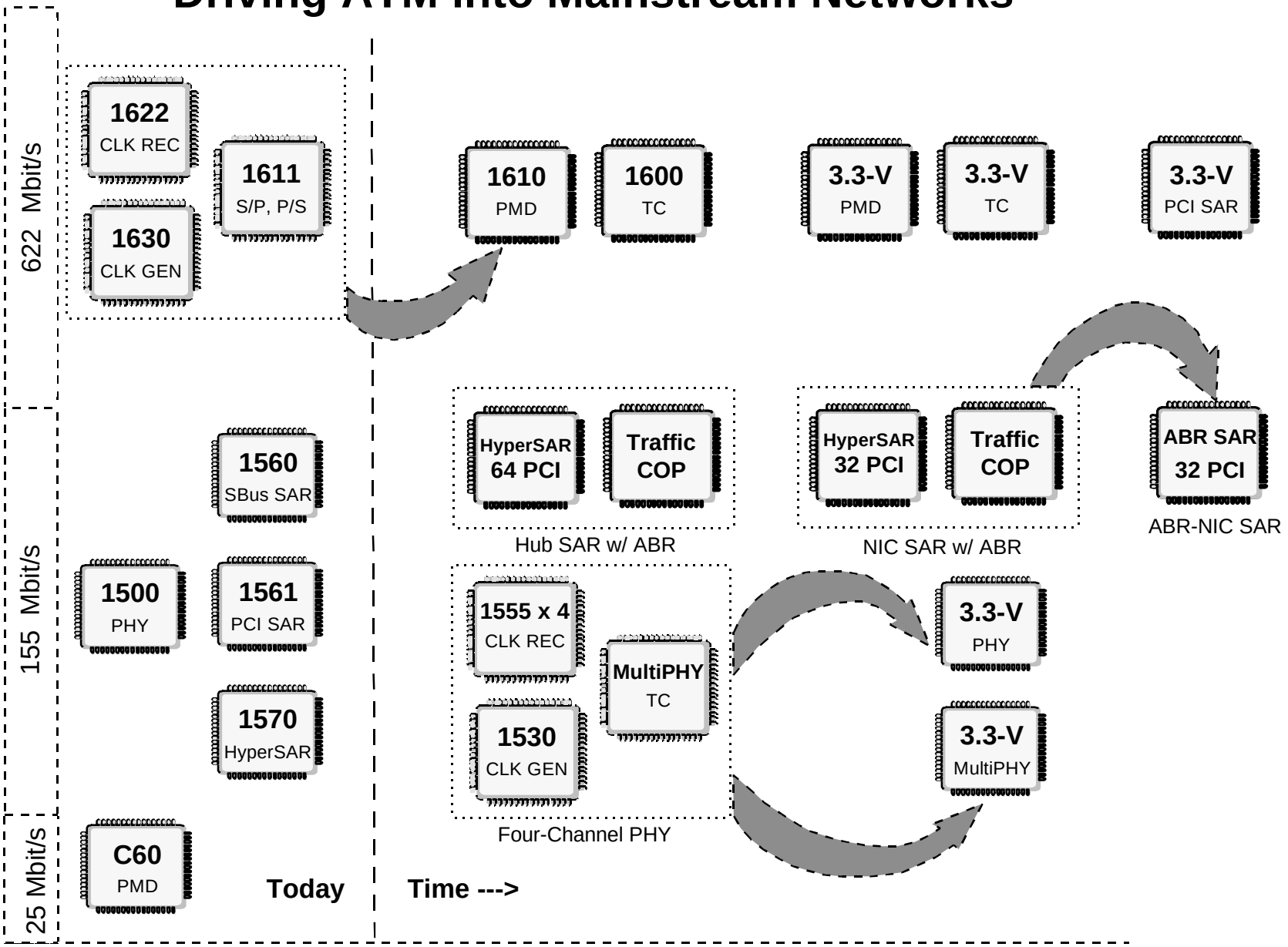
ThunderCELL™ Roadmap

Driving ATM into Mainstream Networks

Driving ATM Into Mainstream Networking



TC = Transmission Convergence
PMD = Physical-Medium Dependent
SAR = Segmentation and Reassembly

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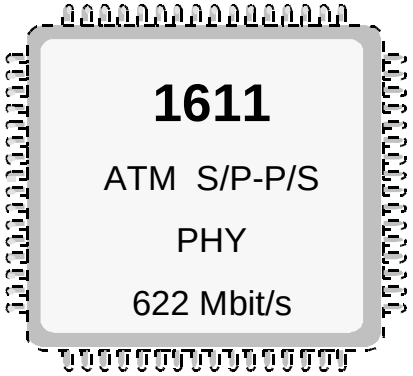
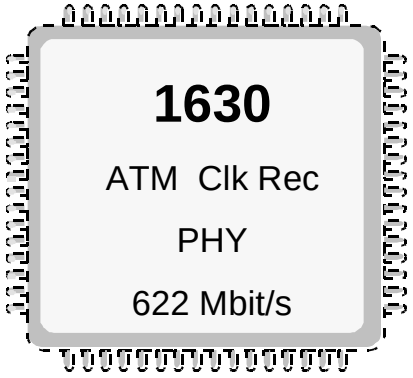
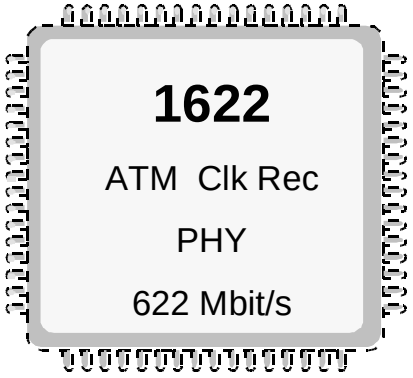
Driving ATM Into Mainstream Networking

622 ThunderCELL™ Family Roadmap to the Future

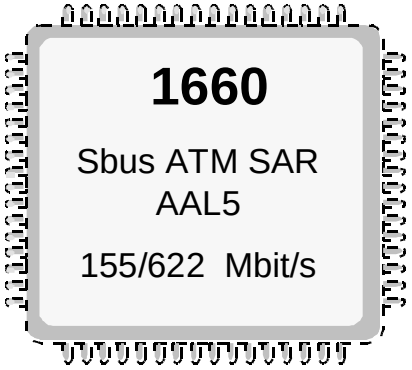
Today

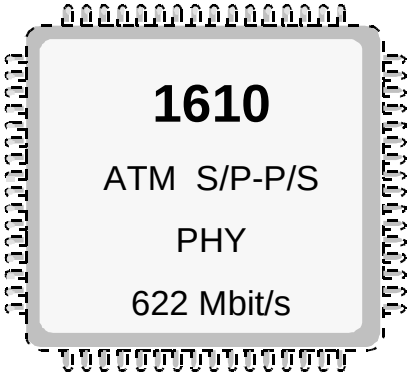


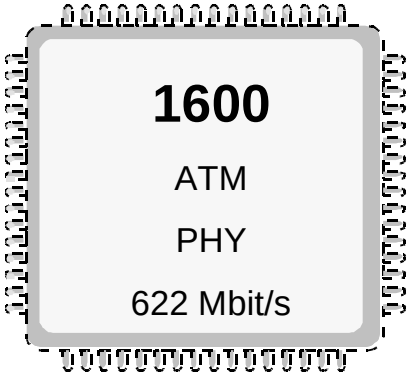




Future







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Driving ATM Into Mainstream Networking

155 ThunderCELL™ Family Roadmap to the Future

Today

1570
PCI ATM SAR
AAL5
200 Mbit/s

1561
PCI ATM SAR
AAL5
155 Mbit/s

1500
ATM PHY
155 Mbit/s

1560
Sbus ATM SAR
AAL5
155 Mbit/s

Future

1505
ATM PHY w/
UTP5 drvr
155 Mbit/s

AAL1 SAR

TRAFFIC MGMT SAR

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TI Solutions

- ATM SAR solutions
- ATM PHY solutions
- Applications
- Evaluation kits
- Contacts

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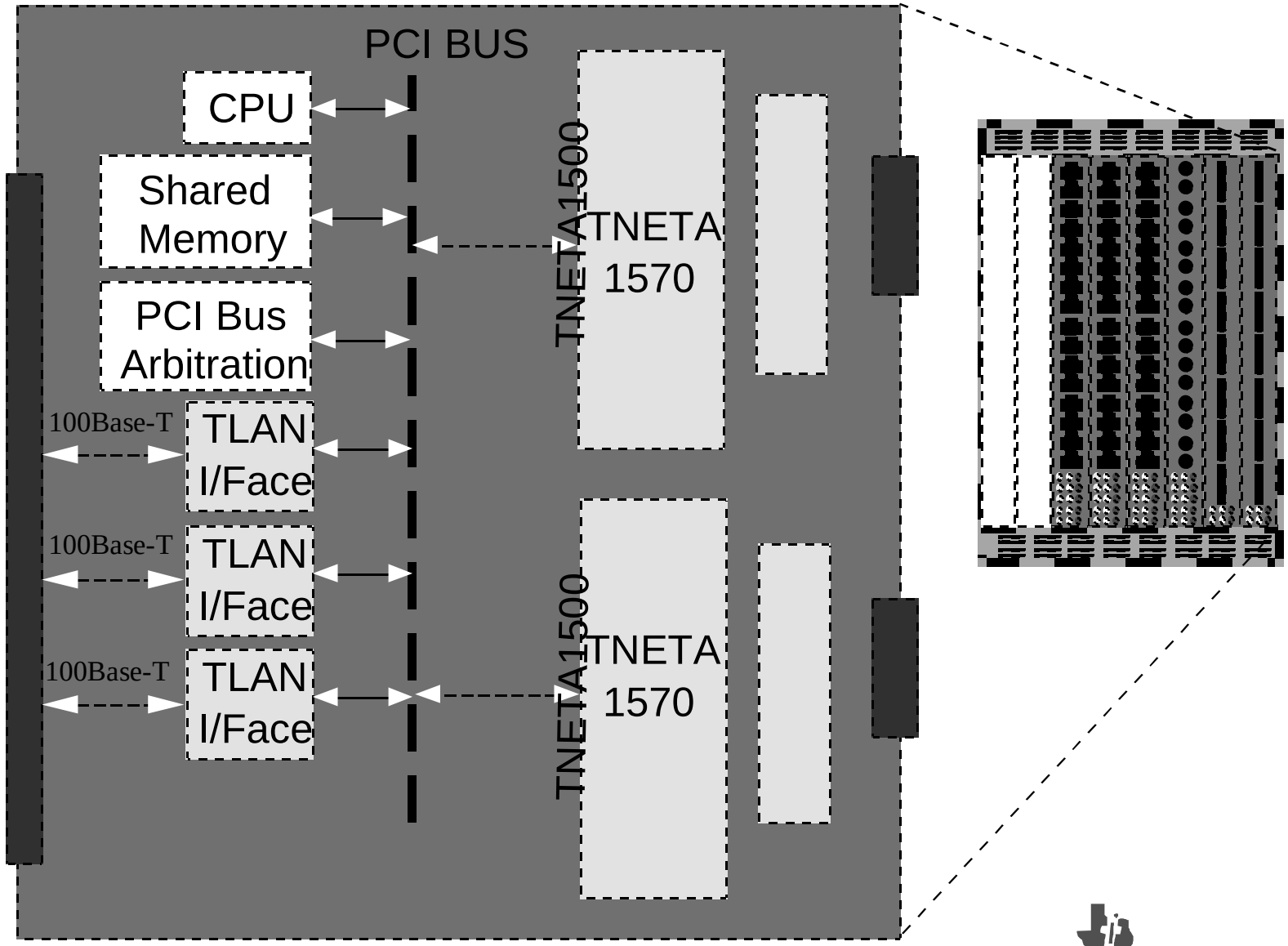
Driving ATM Into Mainstream Networking

Application Enterprise Hub

Frame-Based Backplane Interface to Hub



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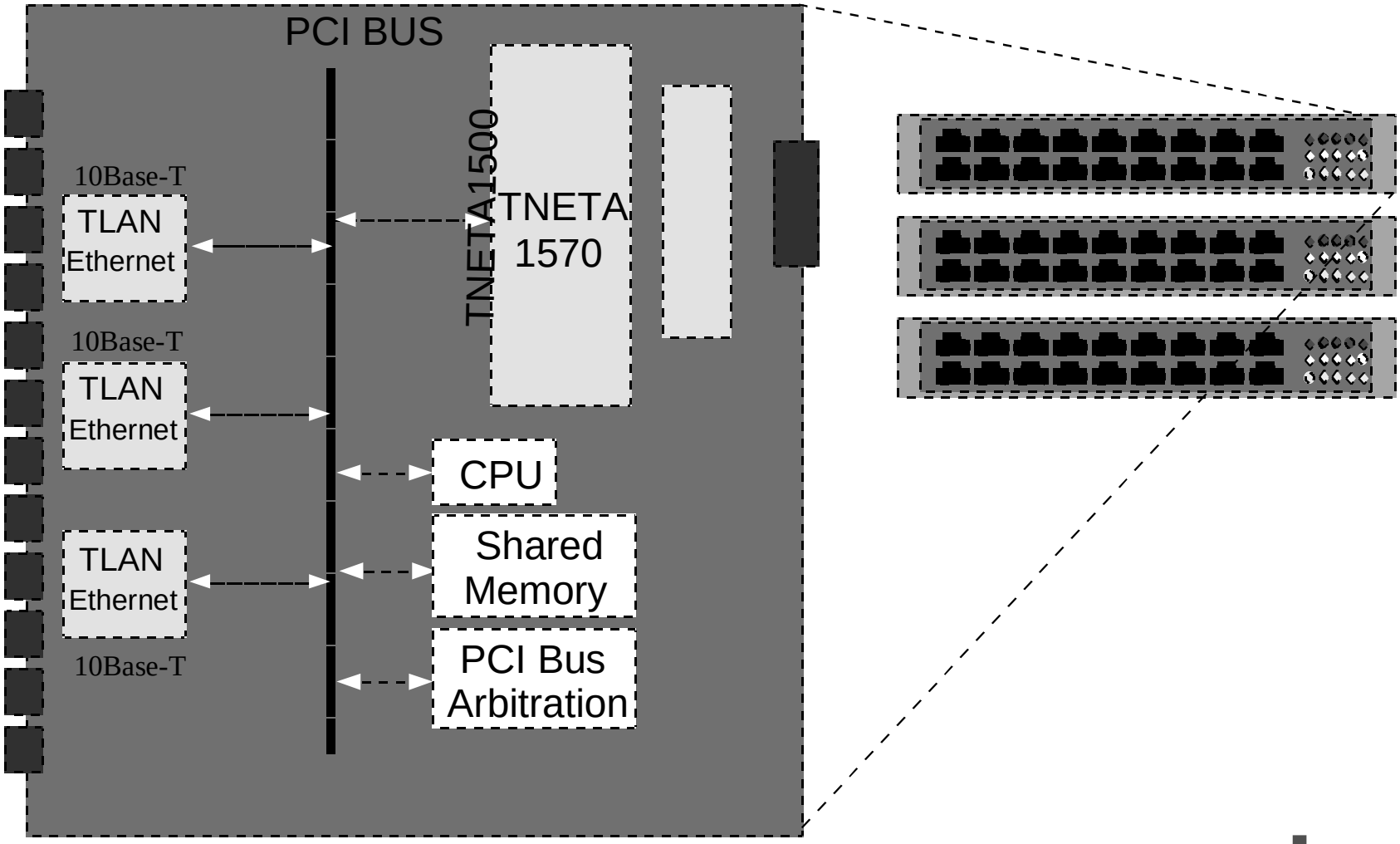
Application Edge Router



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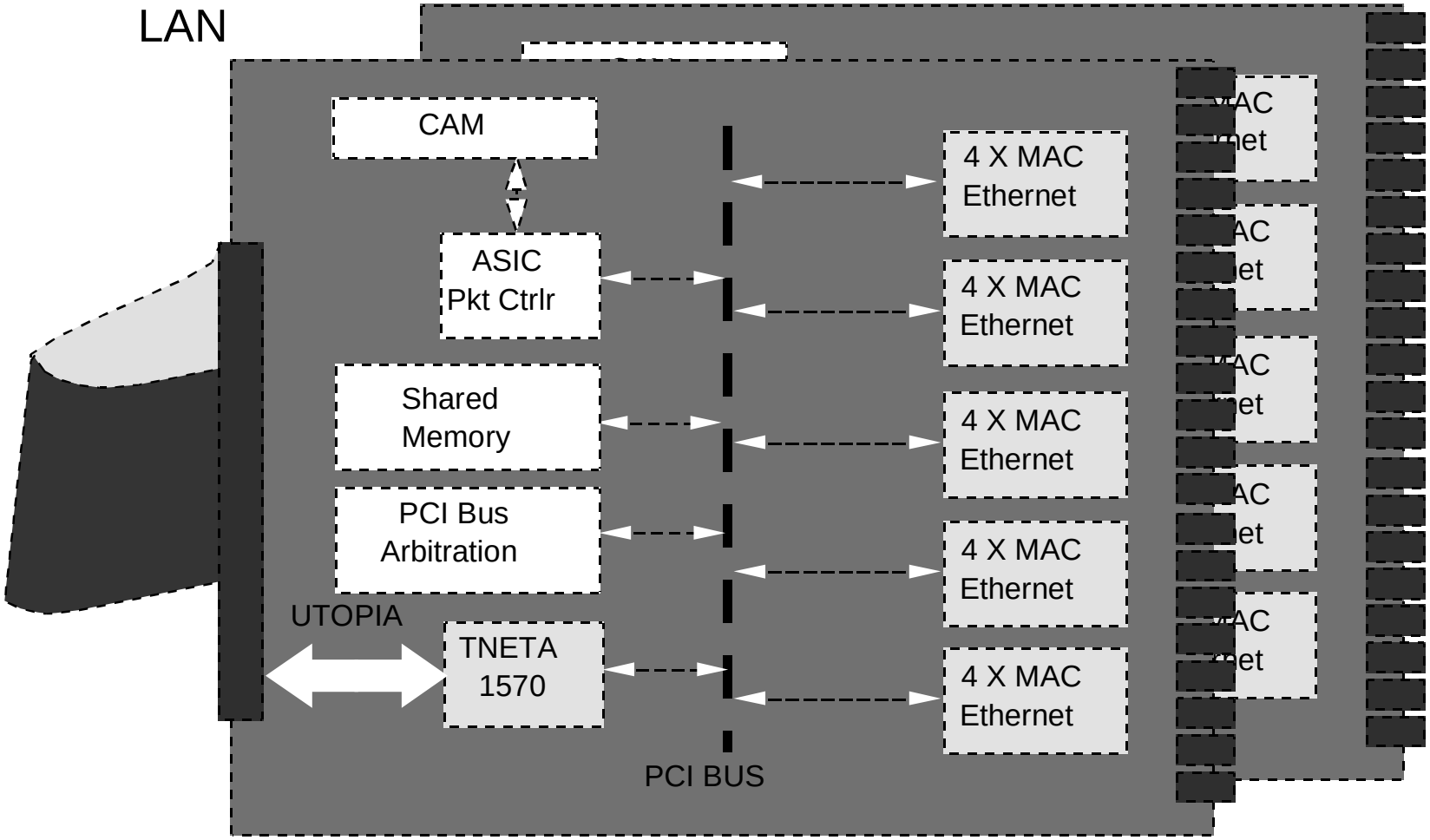
HyperSAR Application
Ethernet Workgroup Switch



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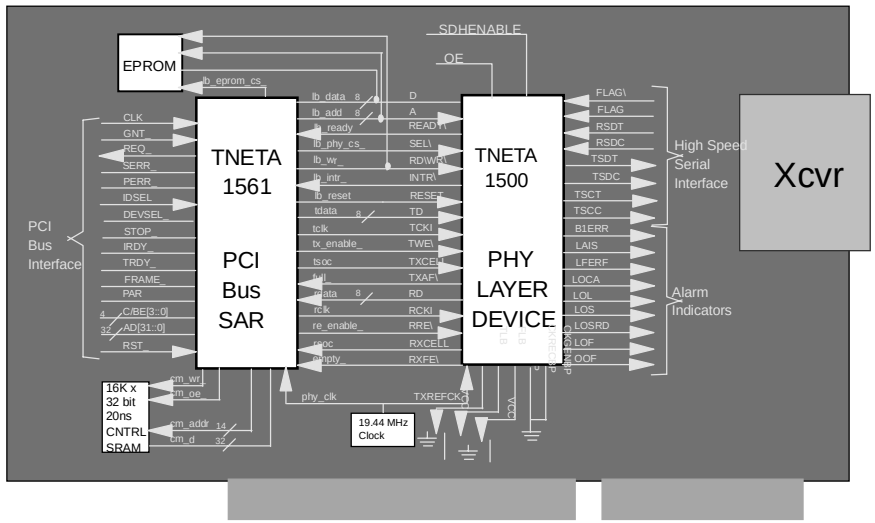
NIC/HUB SAR

TNETA1561

- **FEATURES**
  - **Integated PCI host bus**
  - **Register-based DMA architecture for high performance**
  - **Rx buffer chaining**
- **BENEFITS**
  - **Reduced chip count**
  - **No software overhead to program reduced instruction set computer (RISC) core**
  - **LAN emulation support**



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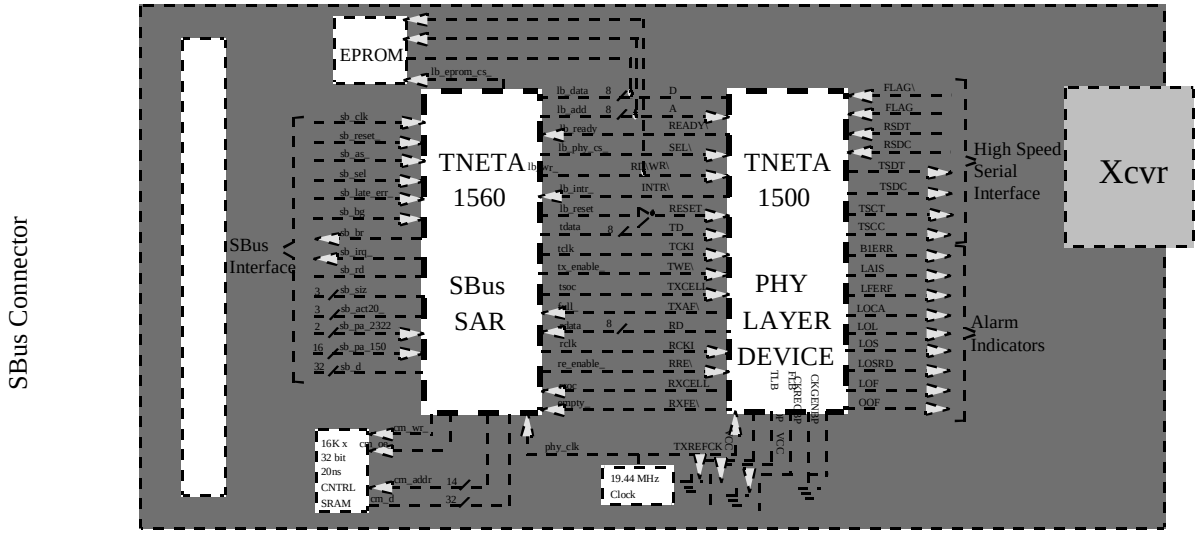
NIC/HUB SAR

TNETA1560

- **FEATURES**
  - **Targeted for adapter card and fat pipe applications**
  - **Integrated S-Bus host bus**
  - **DMA bus mastering**
- **BENEFITS**
  - **Servers and clients needing high-performance ATM connections**
  - **Saves chip count**
  - **Efficient register architecture with no software microcode programming**



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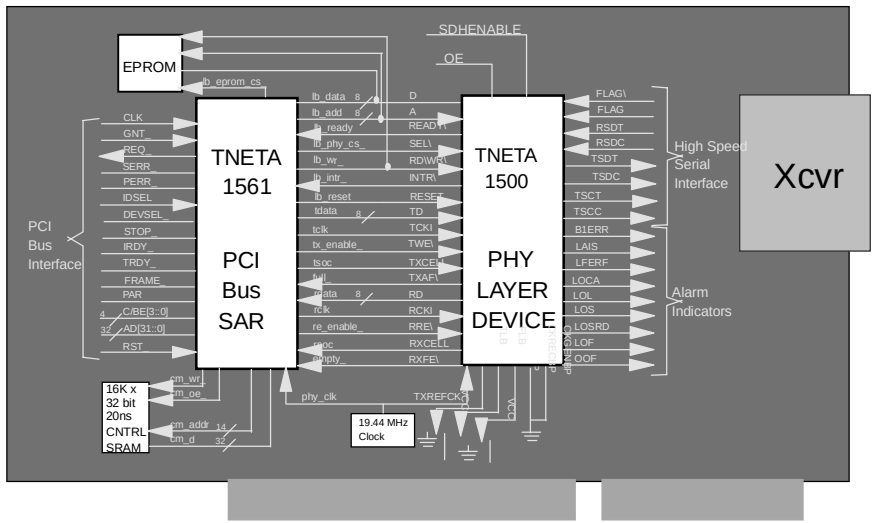
155-Mbit/s ATM PHY

TNETA1500

- **FEATURES**
  - **Integrated clock recovery and clock generation**
  - **Meets UNI 3.1 jitter specs**
  - **Wraparound counters**
- **BENEFITS**
  - **Simpler board for layout**
  - **Customers have compliant systems**
  - **Reduces CPU overhead of saturating counters**



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Switched/Dedicated Ethernet

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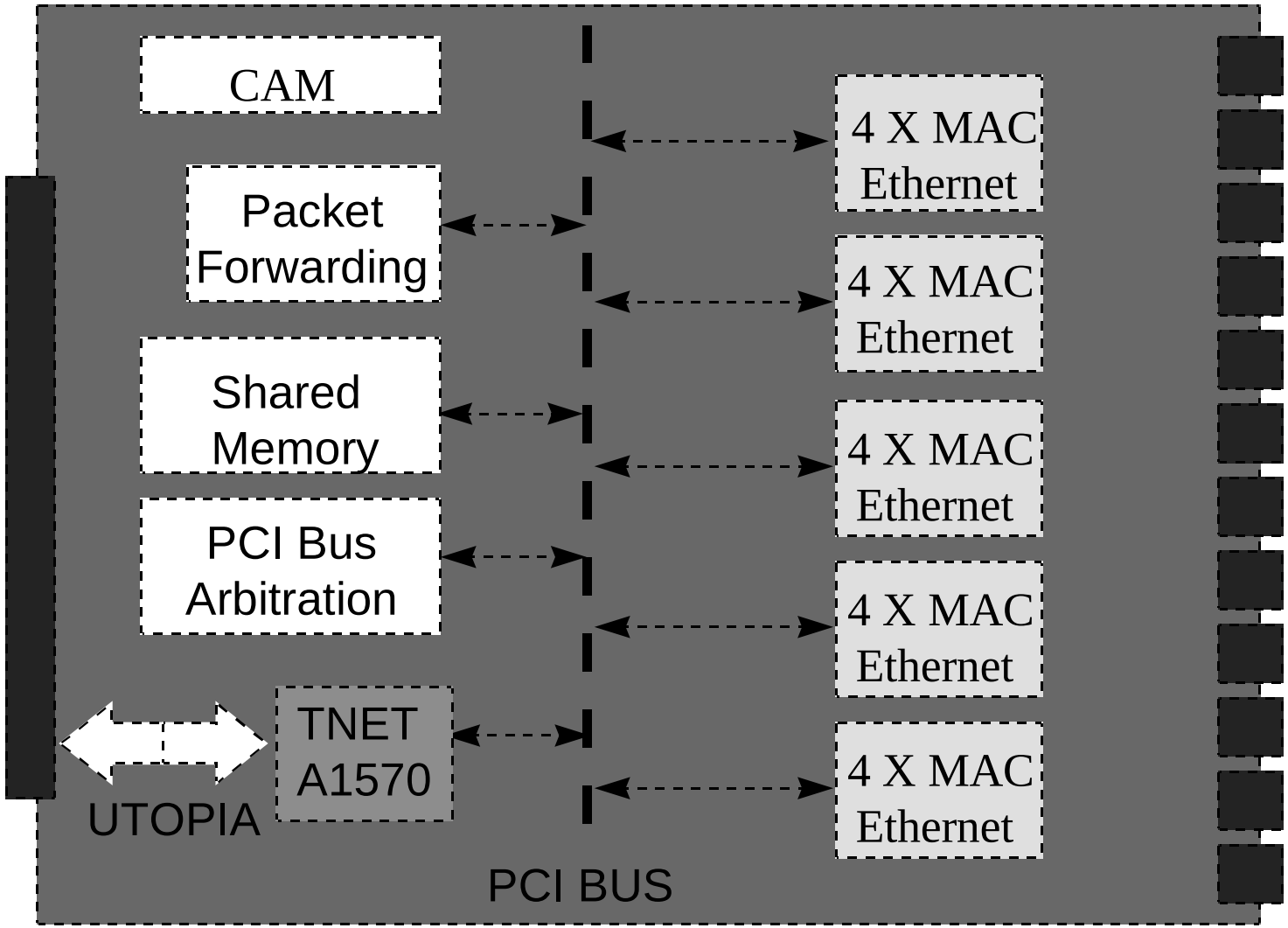

Backplane Interface to ATM Switch

10Base-T Ports

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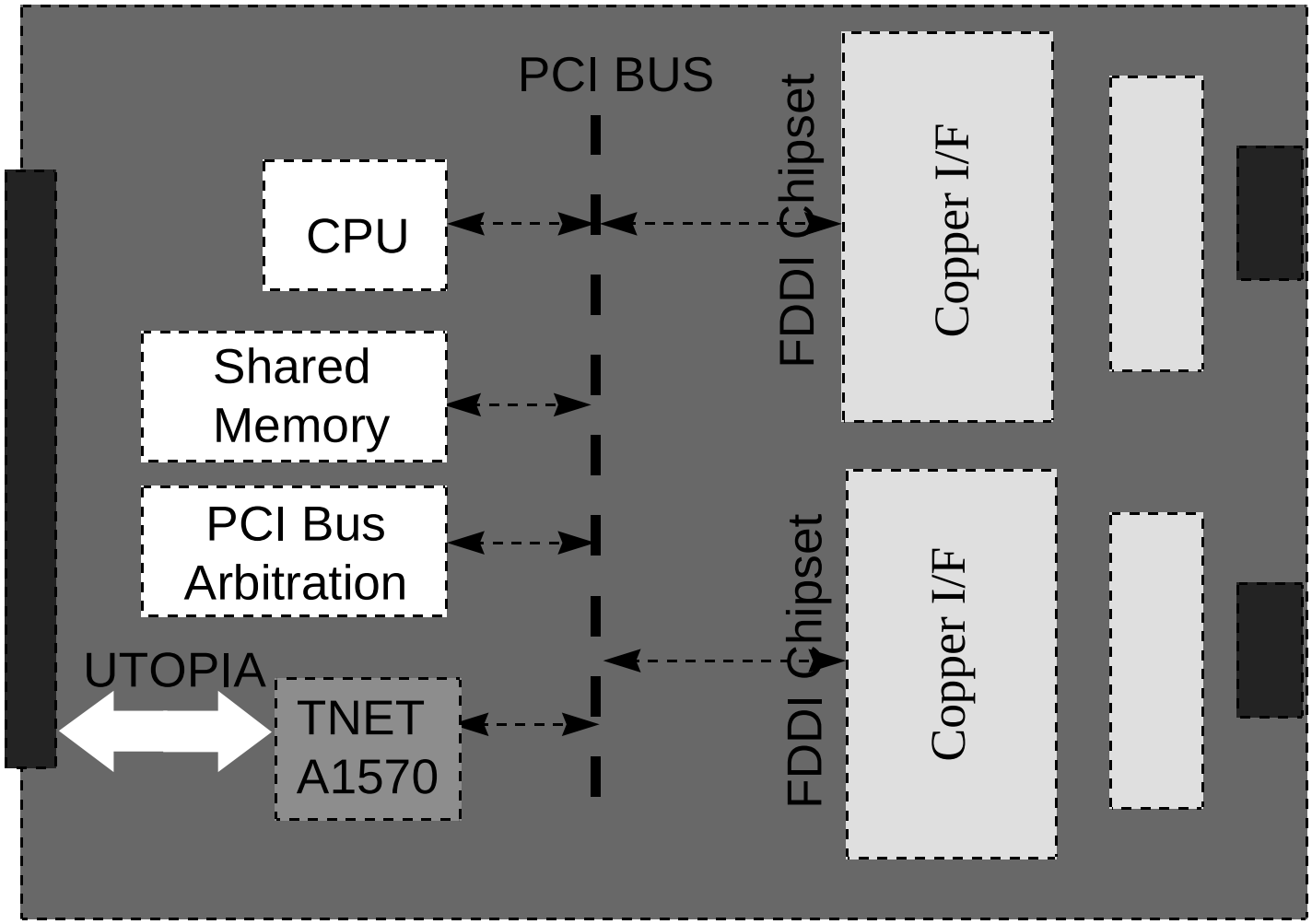
Fiber Distributed Data Interface (FDDI) Card

Backplane Interface to ATM Switch



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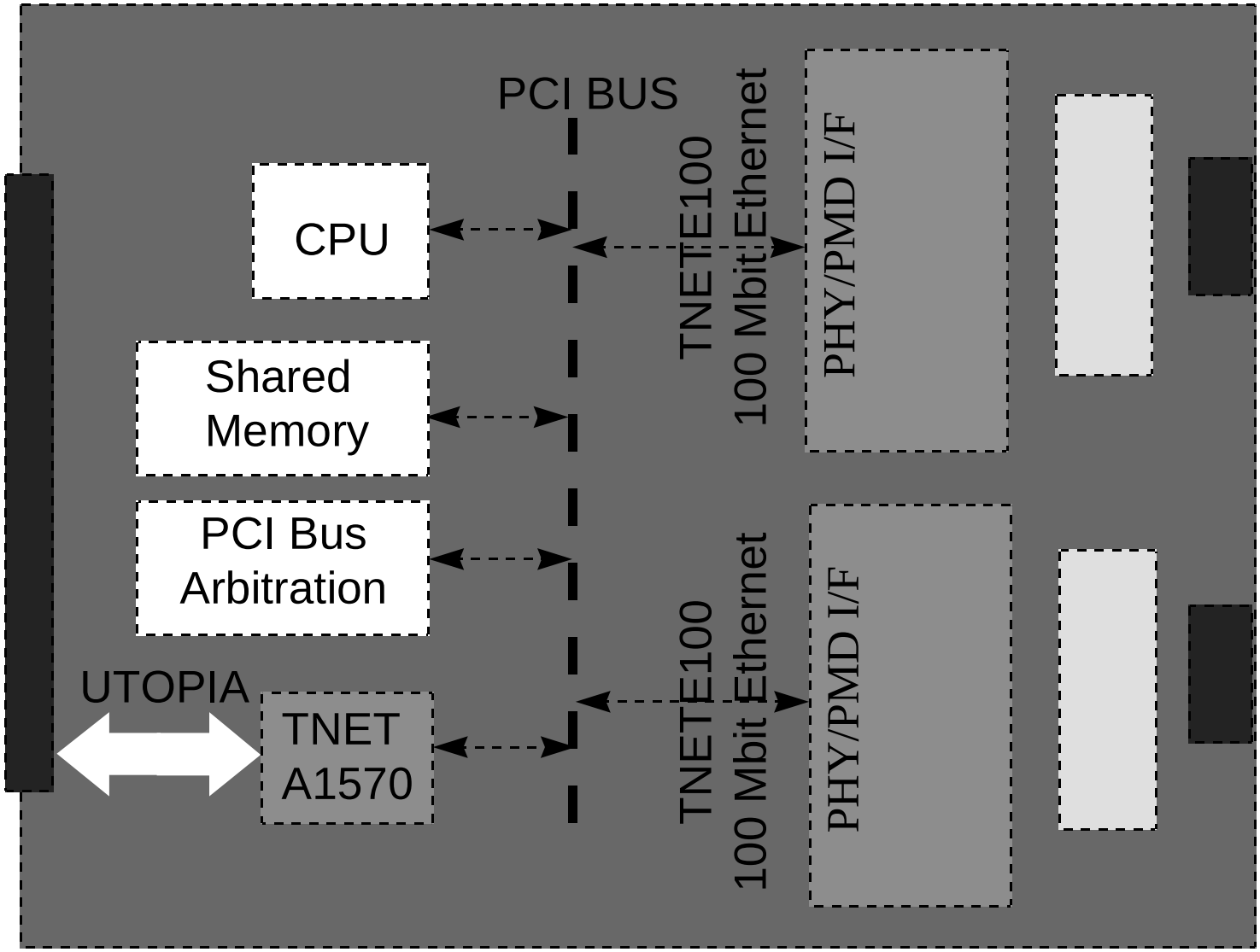
100-Mbit/s Ethernet Interface Card

Backplane Interface to ATM Switch



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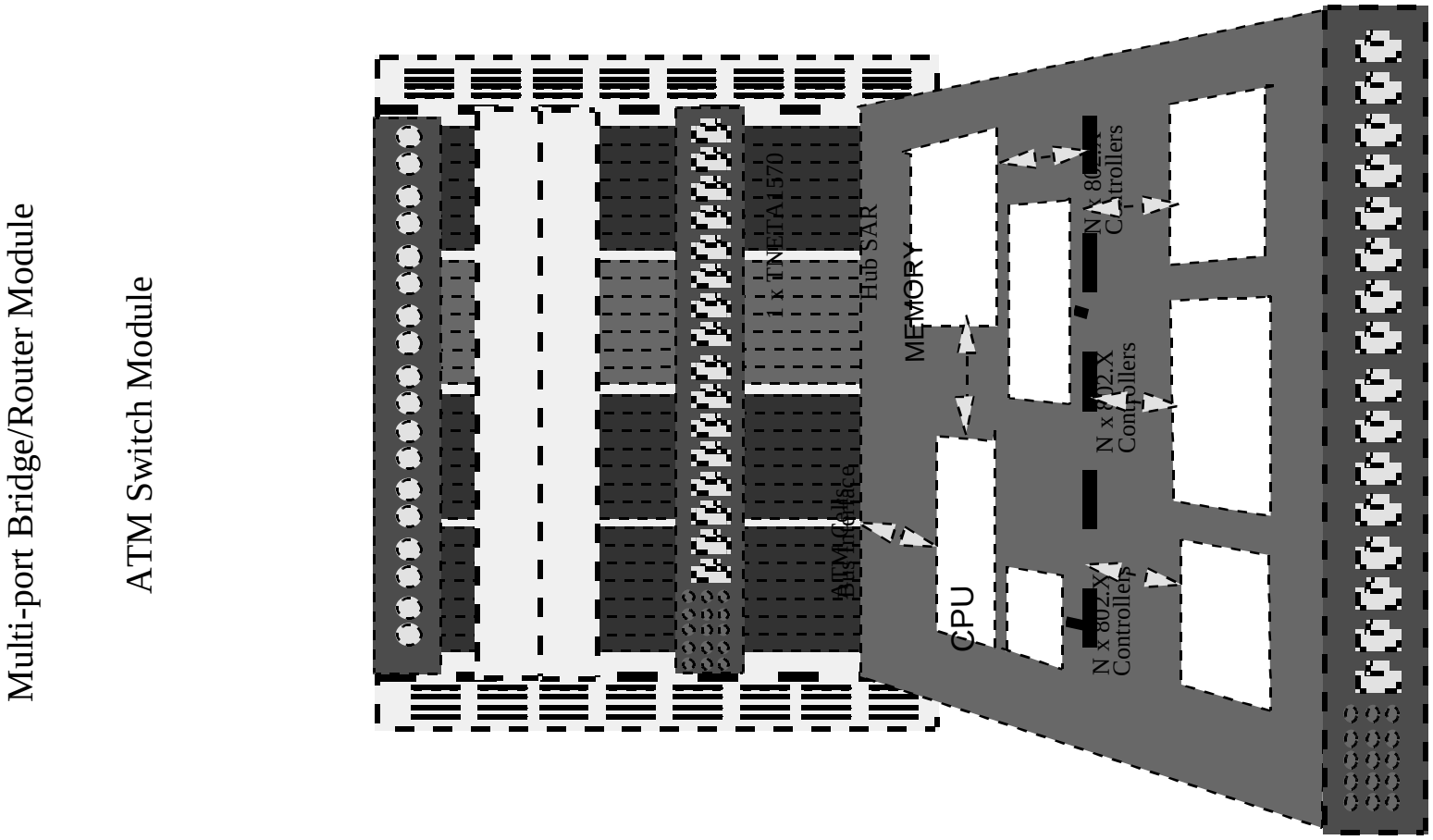
ATM Cell-based Backplane

- More ATM backplanes will be added
- LAN backplanes will move directly to interface cards
- Hub can support switched virtual networks



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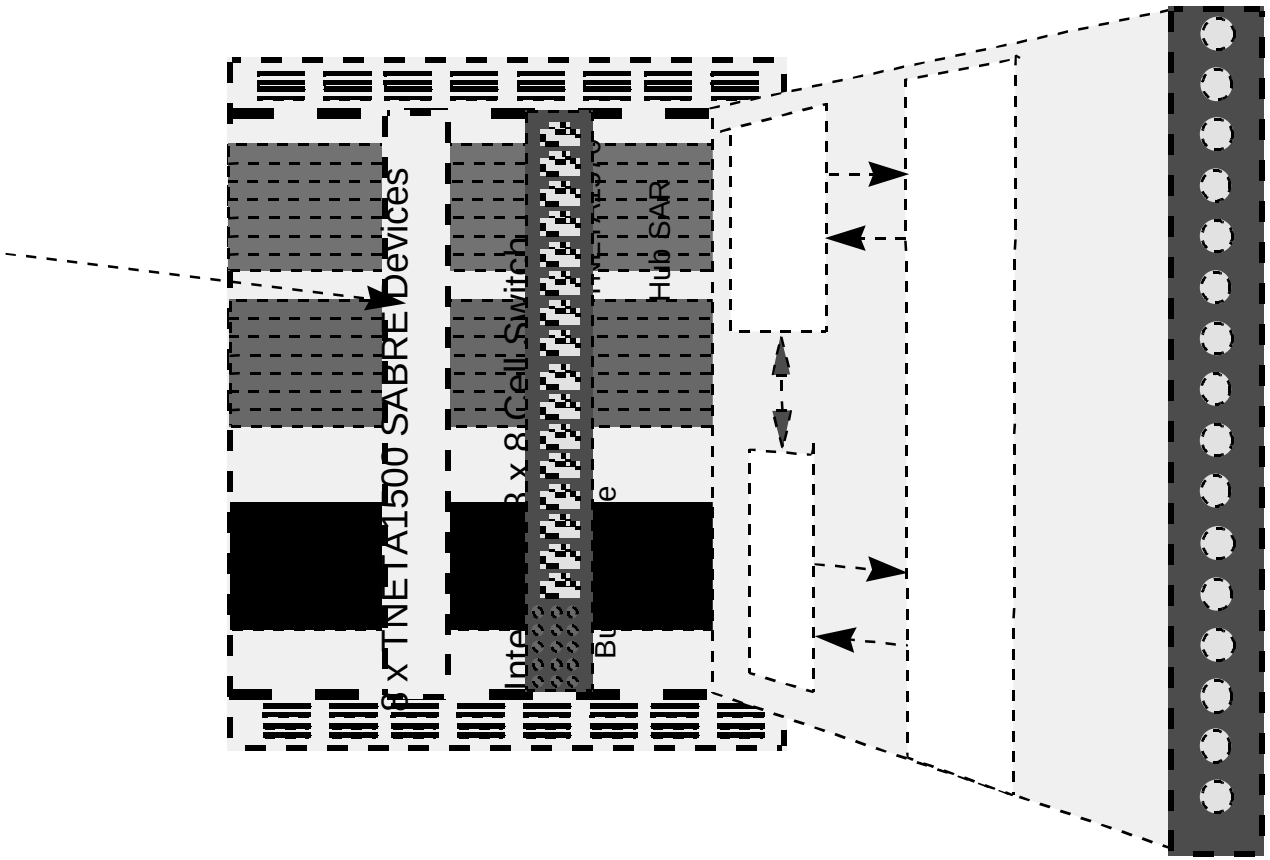
Enterprise Hub With Legacy LAN-Based Backplane

- **Legacy LAN hub with ATM interface card**
- **Allows connection to backbone switch**
- **Provides interfaces for high-performance users**



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TI Solutions

- ATM SAR solutions
- ATM PHY solutions
- Applications
- Evaluation kits
- Contacts

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Designer Kits

- **TI has EVMs available for designers to learn about our SAR products**
- **SARs supported:**
  - **TNETA 1570**
  - **TNETA 1561**
  - **TNETA 1560**
- **Contact TI sales for more details**

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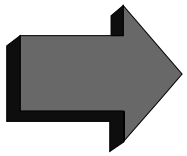

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How to Contact TI

- **E-mail**
  - ***4ATM@msg.ti.com**
- **World-Wide Web**
  - **http://www.ti.com**